# WASP 13 CS
# Whiskey Lake-U

## 2019-01
## REV : A00

*DY : None Installed*
*UMA: UMA only installed*
*OPS: DIS only installed*

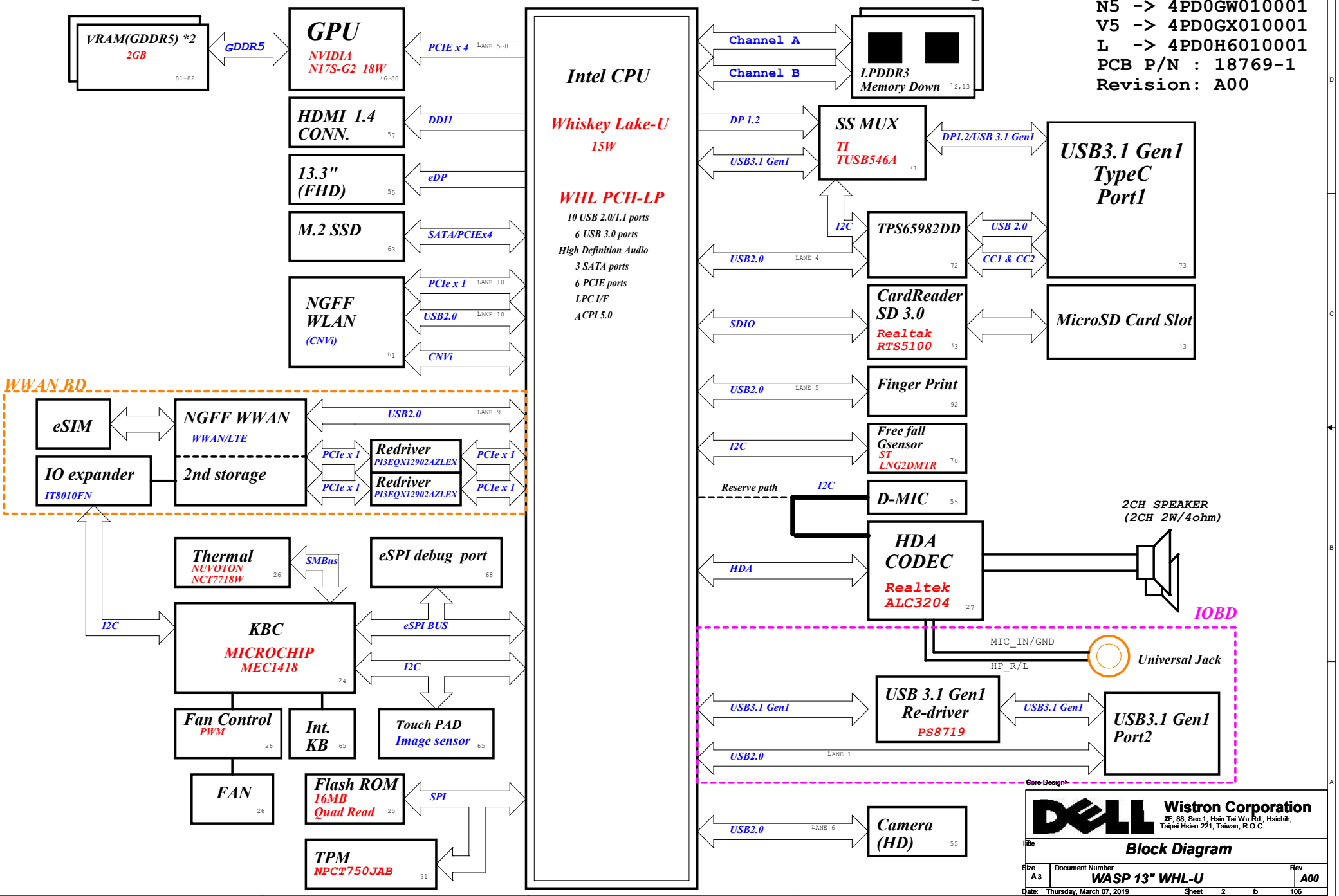
<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

| | | |
|---|---|---|
| Title: Cover Page | | |
| Size: A 4 | Document Number: WASP 13" WHL-U | Rev: A00 |
| Date: Thursday, March 07, 2019 | Sheet 1 of 106 | |

# WASP 13" CPU 15W + GPU 18W Block Diagram

Project code :
N5 -> 4PD0GW010001
V5 -> 4PD0GX010001
L -> 4PD0H6010001
PCB P/N : 18769-1
Revision: A00




Wistron Corporation
2F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Block Diagram

| Size | Document Number | Rev |
|---|---|---|
| A3 | WASP 13" WHL-U | A00 |

Date: Thursday, March 07, 2019 Sheet 2 of 106

WWW.AliSaler.Com

# Main Func = CPU

24 PECI_CPU
24,44,46 PROCHOT#_CPU
55 TOUCH_PANEL_INTR#
24,65 TP_WAKE_KBC#
55 TOUCH_PANEL_PD#
17 H_CPUPWRGD

1V_VCCSTG = 1.05V

[PECI] and [PROCHOT#]
Impedance control: 50 ohm

R301 Rb 1KR2J-1-GP
R302 Ra 499R2F-2-GP
PROCHOT#_CPU

CPU1D 4 OF 20
WHISKEY-LAKE-GP
ZZ.00CPU.271

PECI_CPU AA4
PROCHOT#_CPU_R AR1
THERMTRIP#_CPU Y4
BJ1

CATERR#
PECI
PROCHOT#
THRMTRIP#

TP307 BPM_N0 U1
TP308 BPM_N1 U2
TP302 BPM_CPU_N2 U3
TP303 BPM_CPU_N3 U4

BPM#0
BPM#1
BPM#2
BPM#3

PROC_TCK T6
PROC_TDI U6
PROC_TDO Y5
PROC_TMS T5
PROC_TRST# AB6

PCH_TCK W6
PCH_TDI U5
PCH_TDO W5
PCH_TMS P5
PCH_TRST# Y6
PCH_JTAGX P6

XDP_TCLK → TP309
XDP_TDI → TP310
XDP_TDO_CPU
XDP_TMS
XDP_TRST# → TP313
PCH_TCK → TP314
TP316
TP317

TP304 GPP_E3/CPU_GP0 CE9
TOUCH_PANEL_INTR# CN3
TP_WAKE_KBC# CB34
TOUCH_PANEL_PD# CC35

GPP_E3/CPU_GP0
GPP_E7/CPU_GP1
GPP_B3/CPU_GP2
GPP_B4/CPU_GP3

PROC_PREQ# W2 → XDP_PREQ# → TP305
PROC_PRDY# W1 → XDP_PRDY# → TP306

R304 49D9R2F-GP CPU_POPIRCOMP BP27
R305 49D9R2F-GP PCH_POPIRCOMP BW25

PROC_POPIRCOMP
PCH_OPIRCOMP

3D3V_S5_PCH
R303 DY 100KR2J-1-GP TP_WAKE_KBC#

1V_VCCST_CPU
R308 1KR2J-1-GP THERMTRIP#_CPU

1V_VCCSTG
1V_VCCSTG = 1.05V
R310 51R2J-2-GP XDP_TDO_CPU
R317 51R2J-2-GP XDP_TCLK

THERMTRIP#_CPU
H_CPUPWRGD

ED301 DY
AZ5125-02S-R7G-GP
75.05125.07D

<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (THML/JTAG)
Size: A4
Document Number: WASP 13" WHL-U
Rev: A 00
Date: Thursday, March 07, 2019
Sheet 3 of 106

# Main Func = CPU

## DP to HDMI1.4

57 HDMI_DDI_TX_N0
57 HDMI_DDI_TX_P0
57 HDMI_DDI_TX_N1
57 HDMI_DDI_TX_P1
57 HDMI_DDI_TX_N2
57 HDMI_DDI_TX_P2
57 HDMI_DDI_TX_N3
57 HDMI_DDI_TX_P3

57 HDMI_HPD_CPU

57 CPU_DP1_CTRL_CLK
57 CPU_DP1_CTRL_DATA

## DP for Type-C Mux

71 DP2_DDI_TX_N0
71 DP2_DDI_TX_P0
71 DP2_DDI_TX_N1
71 DP2_DDI_TX_P1
71 DP2_DDI_TX_N2
71 DP2_DDI_TX_P2
71 DP2_DDI_TX_N3
71 DP2_DDI_TX_P3
71 DP2_AUX_CPU_P
71 DP2_AUX_CPU_N

## eDP

55 eDP_TX_CPU_N0
55 eDP_TX_CPU_P0
55 eDP_TX_CPU_N1
55 eDP_TX_CPU_P1

55 eDP_AUX_CPU_N
55 eDP_AUX_CPU_P

55 eDP_HPD_CPU
71,72 DP1_HPD_CPU

24 L_BKLT_EN
55 L_BKLT_CTRL

55 EDP_VDD_EN

15 GPP_H17_STRAP

24 GC6_THM_DIS#

3D3V_S0

20180904 Stuff
R402 1 2 10KR2J-L-GP
SIO_EXT_SMI#

RN401 SRN2K2J-1-GP
CPU_DP1_CTRL_DATA
CPU_DP1_CTRL_CLK

RN403 SRN2K2J-1-GP
CPU_DP2_CTRL_DATA
CPU_DP2_CTRL_CLK

R403 1 2 100KR2J-1-GP
DP1_HPD_CPU_R

3D3V_S5_PCH

RN405 SA 0816 SRN10KJ-5-GP
CPU_DP_HPD_P

Q401 2N7002KDW-1-GP
DP1_HPD_CPU_R
DP1_HPD_CPU

75.27002.F7C

## DP to HDMI

## DP for Type-C Mux

CPU1A 1 OF 20

| | | | |
|---|---|---|---|
| HDMI_DDI_TX_N0 | AL5 | DDI1_TXN0 | EDP_TXN0 AG4 e DP_TX_CPU_N0 |
| HDMI_DDI_TX_P0 | AL6 | DDI1_TXP0 | EDP_TXP0 AG3 e DP_TX_CPU_P0 |
| HDMI_DDI_TX_N1 | AJ5 | DDI1_TXN1 | EDP_TXN1 AG2 e DP_TX_CPU_N1 |
| HDMI_DDI_TX_P1 | AJ6 | DDI1_TXP1 | EDP_TXP1 AG1 e DP_TX_CPU_P1 |
| HDMI_DDI_TX_N2 | AF6 | DDI1_TXN2 | EDP_TXN2 AJ4 |
| HDMI_DDI_TX_P2 | AF5 | DDI1_TXP2 | EDP_TXP2 AJ3 |
| HDMI_DDI_TX_N3 | AE5 | DDI1_TXN3 | EDP_TXN3 AJ2 |
| HDMI_DDI_TX_P3 | AE6 | DDI1_TXP3 | EDP_TXP3 AJ1 |
| DP2_DDI_TX_N0 | AC4 | DDI2_TXN0 | |
| DP2_DDI_TX_P0 | AC3 | DDI2_TXP0 | EDP_AUX_N AH4 e DP_AUX_CPU_N |
| DP2_DDI_TX_N1 | AC1 | DDI2_TXN1 | EDP_AUX_P AH3 e DP_AUX_CPU_P |
| DP2_DDI_TX_P1 | AC2 | DDI2_TXP1 | |
| DP2_DDI_TX_N2 | AE4 | DDI2_TXN2 | DISP_UTILS AM7 |
| DP2_DDI_TX_P2 | AE3 | DDI2_TXP2 | |
| DP2_DDI_TX_N3 | AE1 | DDI2_TXN3 | DDI1_AUX_N AC7 |
| DP2_DDI_TX_P3 | AE2 | DDI2_TXP3 | DDI1_AUX_P AC6 |
| | | | DDI2_AUX_N AD4 D P2_AUX_CPU_N |
| | | | DDI2_AUX_P AD3 D P2_AUX_CPU_P |
| | | | DDI3_AUX_N AG7 |
| | | | DDI3_AUX_P AG6 |
| | | GPP_E13/DDPB_HPD0/DISP_MISC0 | CN6 H DMI_HPD_CPU |
| | | GPP_E14/DDPC_HPD1/DISP_MISC1 | CM6 D P1_HPD_CPU_R |
| | | GPP_E15/DPPD_HPD2/DISP_MISC2 | CP7 S IO_EXT_SMI# |
| | | GPP_E16/DPPE_HPD3/DISP_MISC3 | CP6 |
| | | GPP_E17/EDP_HPD/DISP_MISC4 | CM7 e DP_HPD_CPU |
| | | EDP_BKLTEN | CK11 L_BKLT_EN |
| | | EDP_VDDEN | CG11 E DP_VDD_EN |
| | | EDP_BKLTCTL | CH11 L_BKLT_CTRL |

1 V_VCCIO

R401 1 2 24D9R2F-L-GP
e DP_RCOMP_CPU AM6
DISP_RCOMP

CPU_DP1_CTRL_CLK CC8
CPU_DP1_CTRL_DATA CC9
GPP_E18/DPPB_CTRLCLK/CNV_BT_HOST_WAKE#
GPP_E19/DPPB_CTRLDATA

CPU_DP2_CTRL_CLK CH4
CPU_DP2_CTRL_DATA CH3
GPP_E20/DPPC_CTRLCLK
GPP_E21/DPPC_CTRLDATA

CP4
CN4
GPP_E22/DPPD_CTRLCLK
GPP_E23/DPPD_CTRLDATA

GC6_THM_DIS# CR26
GPP_H17_STRAP CP26
GPP_H16/DDPF_CTRLCLK
GPP_H17/DDPF_CTRLDATA

WHISKEY-LAKE-GP

ZZ.00CPU.271

### (#543016) eDP_RCOMP Guideline

| Signal | Trace Width | Isolation Spacing | Resistor Value | Length |
|---|---|---|---|---|
| eDP_RCOMP | 20 mils | 25 mils | 24.9 □[ □□1% | Max = 100 mils |

### (#543016) DDI Disabling and Termination Guidelines

| Port | Strap | Enable Port | Disable Port |
|---|---|---|---|
| Port 1 | DDPB_CTRLDATA | PU to 3.3 V with 2.2-k □□5% resistor | NC |
| Port 2 | DDPC_CTRLDATA | PU to 3.3 V with 2.2-k □□5% resistor | NC |

<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (DDI/EDP)

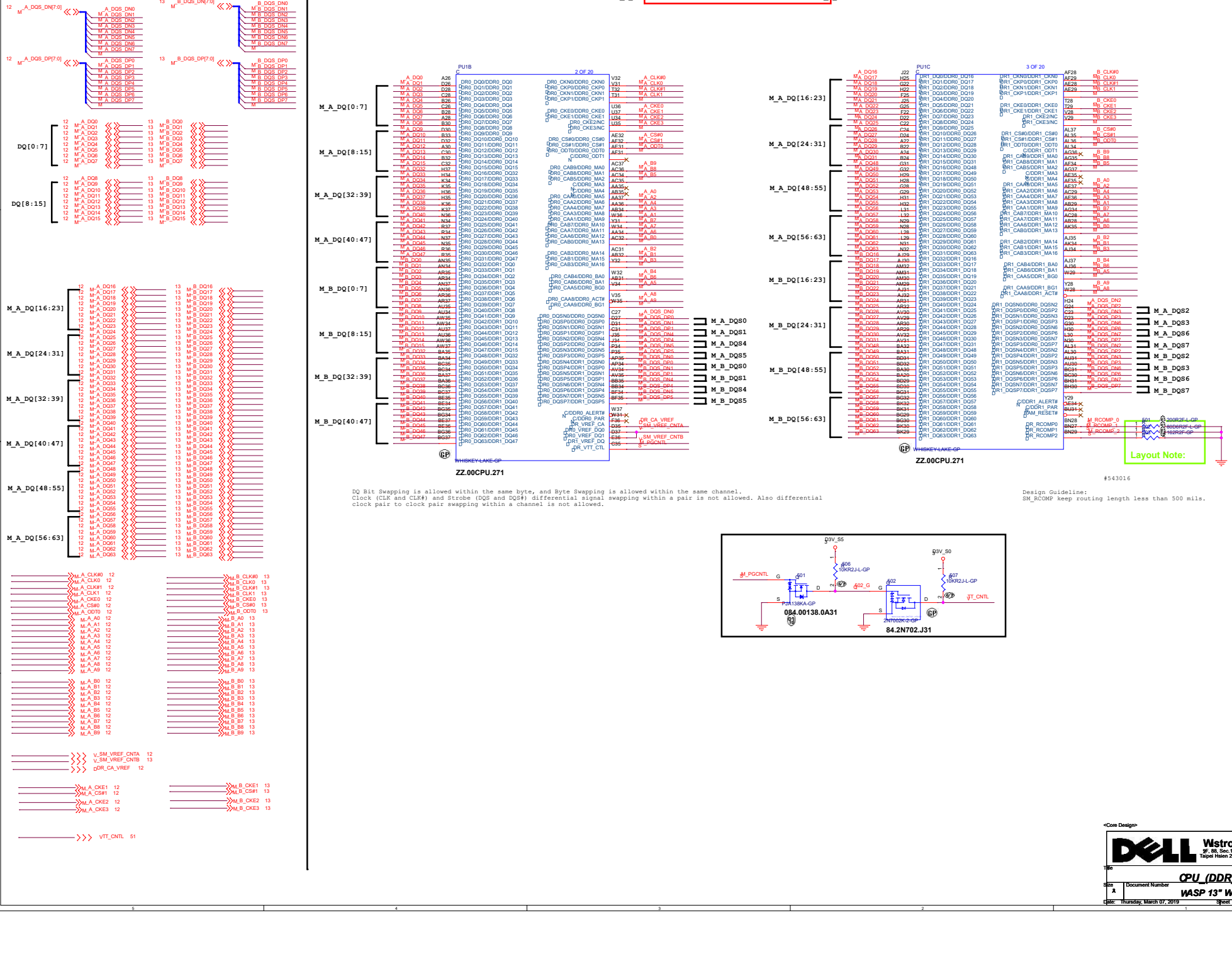
Size: A4 | Document Number: WASP 13" WHL-U | Rev: A00

Date: Thursday, March 07, 2019 | Sheet 4 of 106

WWW.AliSaler.Com

# Main Func = CPU

## DDR4 ball type: Non-Interleaved Type




DQ Bit Swapping is allowed within the same byte, and Byte Swapping is allowed within the same channel.
Clock (CLK and CLK#) and Strobe (DQS and DQS#) differential signal swapping within a pair is not allowed. Also differential clock pair to clock pair swapping within a channel is not allowed.

Design Guideline:
SM_RCOMP keep routing length less than 500 mils.




<Core Design>

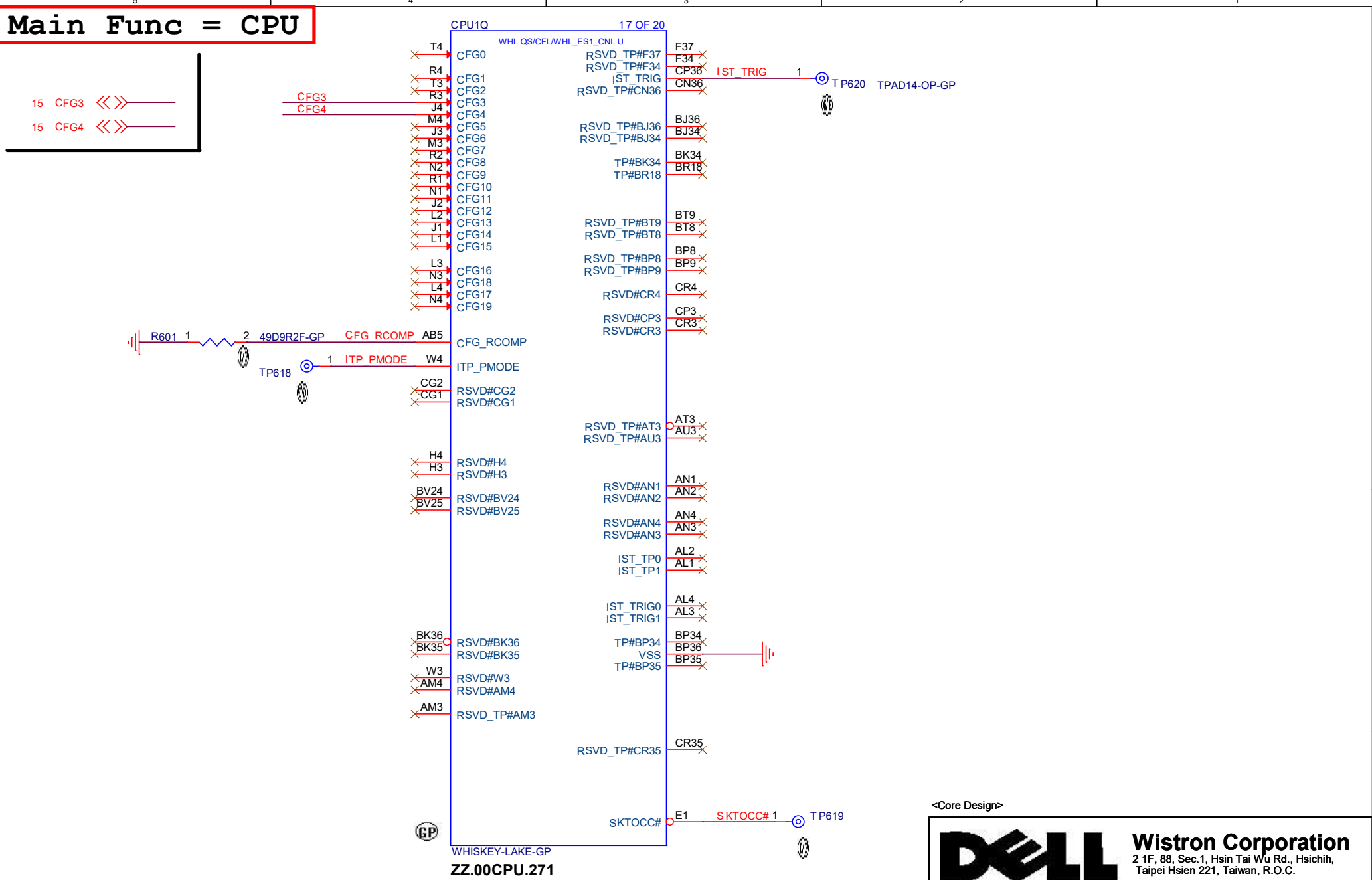
DELL Wistron Corporation
5F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(DDR)

Size: A | Document Number: WASP 13" WHL-U | Rev: A0

Date: Thursday, March 07, 2019 | Sheet 5 of 108

# Main Func = CPU




<Core Design>

**Wistron Corporation**
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

| | | |
|---|---|---|
| Title | CPU (CFG/IST) | |
| Size A4 | Document Number WASP 13" WHL-U | Rev A00 |
| Date: Thursday, March 07, 2019 | Sheet 6 of 106 | |

WWW.AliSaler.Com

# Main Func = CPU

46 VCCCORE_SENSE
46 VSSCORE_SENSE
46 SVID_DATA_CPU
46 SVID_CLK_CPU
46 SVID_ALERT#_CPU

## SVID DATA

1V_VCCST_CPU
#544669
CLOSE TO CPU
R726
100R2F-L1-GP-U
SVID_DATA_CPU_R R709 1 2 0R0402-PAD SVID_DATA_CPU

## SVID CLOCK

1V_VCCST_CPU
#544669
CLOSE TO VR
R723
DY 54D9R2F-L1-GP
SVID_CLK_CPU_R R732 1 2 0R0402-PAD SVID_CLK_CPU

## SVID ALERT

1V_VCCST_CPU
#544669
CLOSE TO CPU
R727
56R2J-4-GP
SVID_ALERT#_CPU_R R728 1 2 220R2J-L2-GP SVID_ALERT#_CPU

## SVID_543016:

Layout Note:
The total Length of Data and Clock (from CPU to each VR) must be equal (□□0.1 inch).
Route the Alert signal between the Clock and the Data signals.

Table 10-10. SVID Bus Routing Guidelines

| Signal | W1 [inches] | W2 [inches] | W3/4/5 [inches] | W2+W3+W4+W5 [inches] | W51 [inches] | W52 [inches] | $R_{pu1}$ [Ω] | $R_{pu2}$ [Ω] | $R_{s1}$ [Ω] | $R_{s2}$ [Ω] | $VCC_{ST}$ [V] |
|---|---|---|---|---|---|---|---|---|---|---|---|
| VIDSOUT | 0.5-3 | 1-15 | 0.5-4 | 3-17 | <0.1 | <0.1 | 100 | 100 | 0 | 10 | 1.0 |
| VIDSCK | | | | | | | Empty | 45 | 0 | 50 | |
| VIDALERT# | | | | | | | 56 | Empty | 220 | 0 | |

1V_CPU_CORE
CPU1L
1 2 OF 20
1V_CPU_CORE

| | | | |
|---|---|---|---|
| AN9 | VCCCORE | VCCCORE | AW24 |
| AN10 | VCCCORE | VCCCORE | AW25 |
| AN24 | VCCCORE | VCCCORE | AW26 |
| AN26 | VCCCORE | VCCCORE | AW27 |
| AN27 | VCCCORE | VCCCORE | AY24 |
| AP2 | VCCCORE | VCCCORE | AY26 |
| AP9 | VCCCORE | VCCCORE | BA5 |
| AP24 | VCCCORE | VCCCORE | BA7 |
| AP26 | VCCCORE | VCCCORE | BA8 |
| AR5 | VCCCORE | VCCCORE | BA25 |
| AR6 | VCCCORE | VCCCORE | BA27 |
| AR7 | VCCCORE | VCCCORE | BB2 |
| AR8 | VCCCORE | VCCCORE | BB26 |
| AR10 | VCCCORE | VCCCORE | BC5 |
| AR25 | VCCCORE | VCCCORE | BC6 |
| AR27 | VCCCORE | VCCCORE | BC7 |
| AT9 | VCCCORE | VCCCORE | BC9 |
| AT24 | VCCCORE | VCCCORE | BC10 |
| AT26 | VCCCORE | VCCCORE | BC26 |
| AU5 | VCCCORE | VCCCORE | BC27 |
| AU6 | VCCCORE | VCCCORE | BD5 |
| AU7 | VCCCORE | VCCCORE | BD8 |
| AU8 | VCCCORE | VCCCORE | BD10 |
| AU9 | VCCCORE | VCCCORE | BD25 |
| AU24 | VCCCORE | VCCCORE | BD27 |
| AU25 | VCCCORE | VCCCORE | BE9 |
| AU26 | VCCCORE | VCCCORE | BE24 |
| AU27 | VCCCORE | VCCCORE | BE25 |
| AV2 | VCCCORE | VCCCORE | BE26 |
| AV5 | VCCCORE | VCCCORE | BE27 |
| AV7 | VCCCORE | VCCCORE | BF2 |
| AV10 | VCCCORE | VCCCORE | BF9 |
| AV27 | VCCCORE | VCCCORE | BF24 |
| AW5 | VCCCORE | VCCCORE | BF26 |
| AW6 | VCCCORE | VCCCORE | BG27 |
| AW7 | VCCCORE | VCCCORE | |
| AW8 | VCCCORE | | |
| AW9 | VCCCORE | VCC_SENSE | AN6 V CCCORE_SENSE |
| AW10 | VCCCORE | VSS_SENSE | AN5 V SSCORE_SENSE |
| | VCCCORE | VIDALERT# | AA3 S VID_ALERT#_CPU_R |
| BB9 | RSVD#BB9 | VIDSCK | AA1 S VID_CLK_CPU_R |
| BC24 | RSVD#BC24 | VIDSOUT | AA2 S VID_DATA_CPU_R |
| AY9 | RSVD#AY9 | RSVD#Y3 | Y3 |
| BB24 | RSVD#BB24 | VCCSTG | BG3 |

1 V_VCCSTG

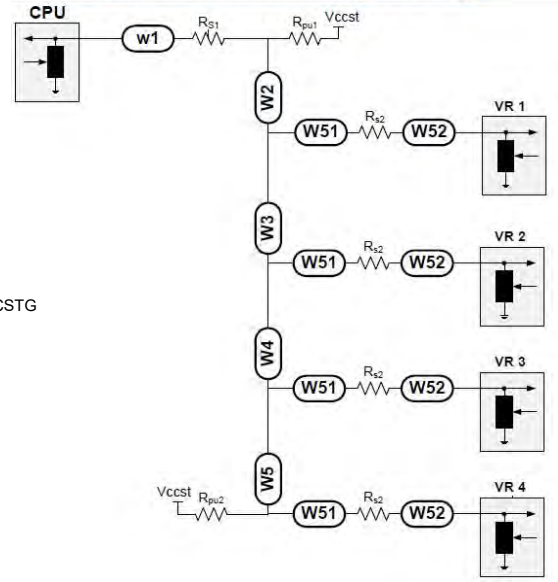
WHISKEY-LAKE-GP
**ZZ.00CPU.271**

1 V_CPU_CORE
R 719
100R2F-L1-GP-U
V CCCORE_SENSE
V SSCORE_SENSE
R 720
100R2F-L1-GP-U

**Layout Note:**

1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Length match<25mil

Figure 10-7. Routing Illustration for SVID Topology




<Core Design>

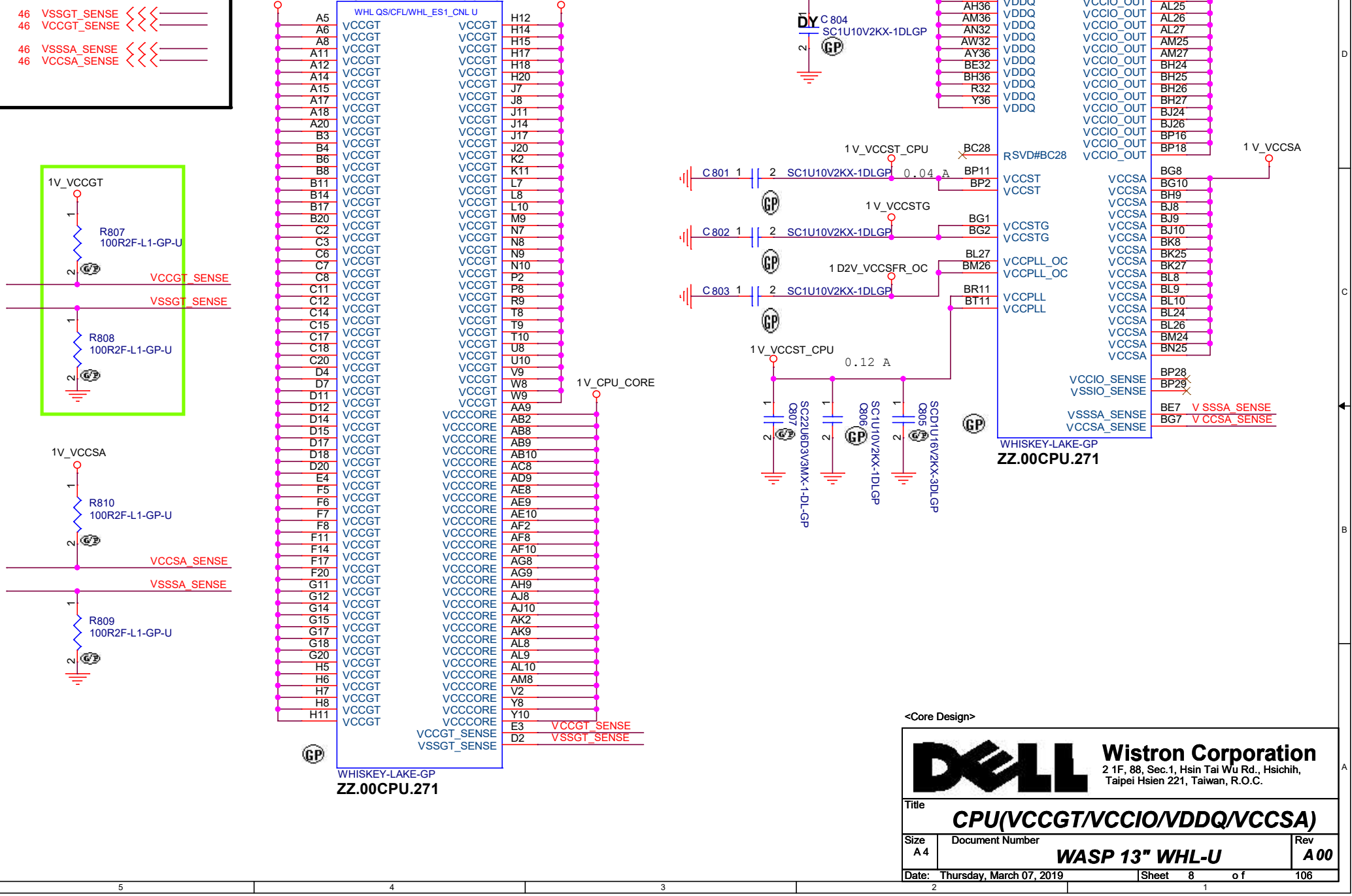
Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (VCORE/VID)**

| Size | Document Number | Rev |
|---|---|---|
| A 4 | WASP 13" WHL-U | A 00 |

Date: Thursday, March 07, 2019 Sheet 7 of 106

# Main Func = CPU




<Core Design>

**Wistron Corporation**
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU(VCCGT/VCCIO/VDDQ/VCCSA)**

| Size | Document Number | Rev |
|---|---|---|
| A 4 | WASP 13" WHL-U | A 00 |

Date: Thursday, March 07, 2019 Sheet 8 of 106

WWW.AliSaler.Com

# (Blanking)

<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

*(Reserved)*

| Size | Document Number | Rev |
|---|---|---|
| A4 | *WASP 13" WHL-U* | *A00* |

Date: Thursday, March 07, 2019 Sheet 9 of 106

# Main Func = CPU

## 1V_CPU_CORE

1V_CPU_CORE

22U 0603 x 39 (7DY)

PC1002 PC1003 PC1004 PC1005 PC1006 PC1007 PC1008 PC1009 PC1010 PC1011 PC1012 PC1013 PC1014 PC1015 PC1016 PC1017 PC1018 PC1019 PC1020 PC1021
U42 U42 U42 U42 U42 U42 U42 U42 U42 U42 U42 U42 U42

SC22U6D3V3MX-1-DL-GP
SC22U6D3V3MX-1-DL-GP
SC22U6D3V3MX-1-DL-GP
SC22U6D3V3MX-1-DL-GP

PC1022 PC1023 PC1024 PC1025 PC1026 PC1027 PC1028 PC1029 PC1030 PC1031 PC1032 PC1034 PC1036 PC1079 PC1080 PC1081 PC1082 PC1083 PC1084
DY DY U42 DY U42 DY DY DY DY DY U42

SC22U6D3V3MX-1-DL-GP
SC22U6D3V3MX-1-DL-GP
SC22U6D3V3MX-1-DL-GP
SC22U6D3V3MX-1-DL-GP

## VCCGT

1V_VCCGT

22U 0603 x 35 (9 DY)

PC1037 PC1038 PC1039 PC1040 PC1041 PC1042 PC1043 PC1044 PC1045 PC1046 PC1047 PC1048 PC1049 PC1050 PC1051 PC1052 PC1053 PC1054 PC1055 PC1056
DY

SC22U6D3V3MX-1-DL-GP
SC22U6D3V3MX-1-DL-GP
SC22U6D3V3MX-1-DL-GP
SC22U6D3V3MX-1-DL-GP

PC1057 PC1058 PC1059 PC1060 PC1061 PC1062 PC1063 PC1064
DY DY DY

SC22U6D3V3MX-1-DL-GP
SC22U6D3V3MX-1-DL-GP
SC22U6D3V3MX-1-DL-GP
SC22U6D3V3MX-1-DL-GP

PC1065 PC1066 PC1067 PC1068 PC1069 PC1070 PC1001
DY DY DY DY DY DY

SC22U6D3V3MX-1-DL-GP
SC22U6D3V3MX-1-DL-GP
SC22U6D3V3MX-1-DL-GP
SC22U6D3V3MX-1-DL-GP

## VCCSA

1V_VCCSA

22U 0603 x 8 (3DY)

PC1071 PC1072 PC1073 PC1074 PC1075 PC1076 PC1077 PC1078
DY DY DY

SC22U6D3V3MX-1-DL-GP
SC22U6D3V3MX-1-DL-GP
SC22U6D3V3MX-1-DL-GP
SC22U6D3V3MX-1-DL-GP

<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(Power CAP1)

Size: A4 | Document Number: WASP 13" WHL-U | Rev: A 00

Date: Thursday, March 07, 2019 | Sheet 10 of 106

WWW.AliSaler.Com

# Main Func = CPU

## PCH DERIVED RAILS

1D0V_S5

C1112 C1128 C1129

SC22U6D3V3MX-1-DL-GP
SC22U6D3V3MX-1-DL-GP
SC22U6D3V3MX-1-DL-GP

3D3V_S5_PCH — R1103 (0R0603-PAD) — 3D3V_VCCPRIM

C1113 SC22U6D3V3MX-1-DL-GP

1D8V_S5 — R1104 (0R0603-PAD) — 1D8V_VCCPRIM

C1122 SC22U6D3V3MX-1-DL-GP

3D3V_VCCPRIM

C1123 SC10U6D3V3MX-DL-GP

## UNSLICED GT

1V_VCCGT

1U 0402 x 6

C1102 C1103 C1104 C1105 C1106 C1107

SC1U10V2KX-1DLGP
SC1U10V2KX-1DLGP
SC1U10V2KX-1DLGP

SC1U10V2KX-1DLGP
SC1U10V2KX-1DLGP
SC1U10V2KX-1DLGP

## VCCIO

1V_VCCIO

+VCCIO(ICCMAX.=2.73A)

C1133 C1134 C1135

SC22U6D3V3MX-1-DL-GP
SC22U6D3V3MX-1-DL-GP
SC22U6D3V3MX-1-DL-GP

C1108 C1109 C1110 C1111

SC1U10V2KX-1DLGP
SC1U10V2KX-1DLGP
SC1U10V2KX-1DLGP
SC1U10V2KX-1DLGP

+VCCMPHYGTAON_1P0(ICCMAX.=2.12A)

1D0V_S5 — C1115 SC22U6D3V3MX-1-DL-GP; C1114 SC1U10V2KX-1DLGP

1D0V_S5 — C1116 C1117

SC1U10V2KX-1DLGP
SC1U10V2KX-1DLGP

1D0V_S5 — C1118 SC22U6D3V3MX-1-DL-GP; C1119 SC1U10V2KX-1DLGP

1D0V_S5 — C1120 SC10U6D3V3MX-DL-GP; C1121 SC1U10V2KX-1DLGP

1D2V_S3

C1132 C1131 C1130

SC22U6D3V3MX-1-DL-GP
SC22U6D3V3MX-1-DL-GP
SC22U6D3V3MX-1-DL-GP

C1136 C1137 C1138

SC10U6D3V3MX-DL-GP
SC10U6D3V3MX-DL-GP
SC10U6D3V3MX-DL-GP

C1139 C1140 C1141 C1142

SCD1U16V2KX-3DLGP
SCD1U16V2KX-3DLGP
SCD1U16V2KX-3DLGP
SCD1U16V2KX-3DLGP

<Core Design>

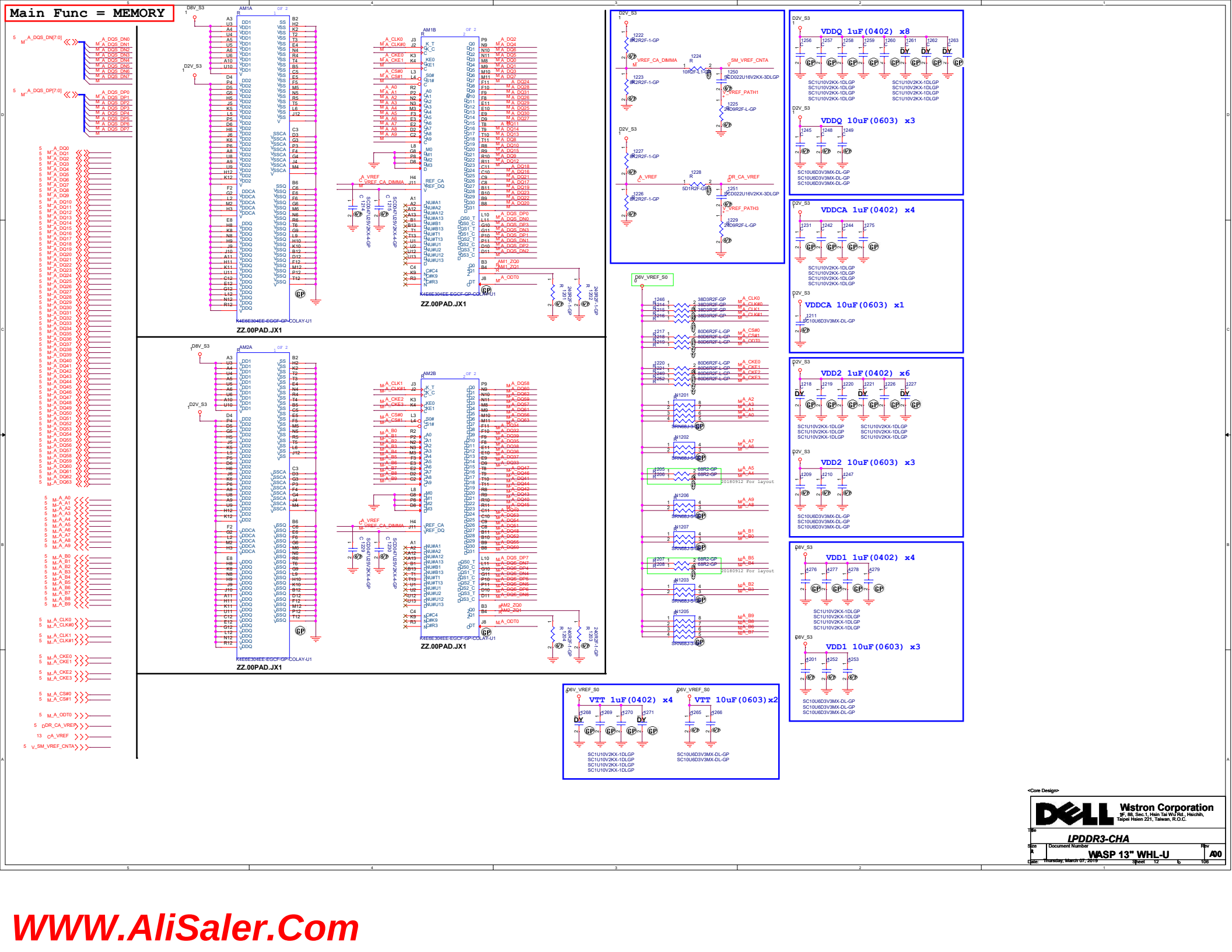
Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(Power CAP2)

Size: A4 | Document Number: WASP 13" WHL-U | Rev: A 00

Date: Thursday, March 07, 2019 | Sheet 11 of 106

# Main Func = MEMORY




WWW.AliSaler.Com

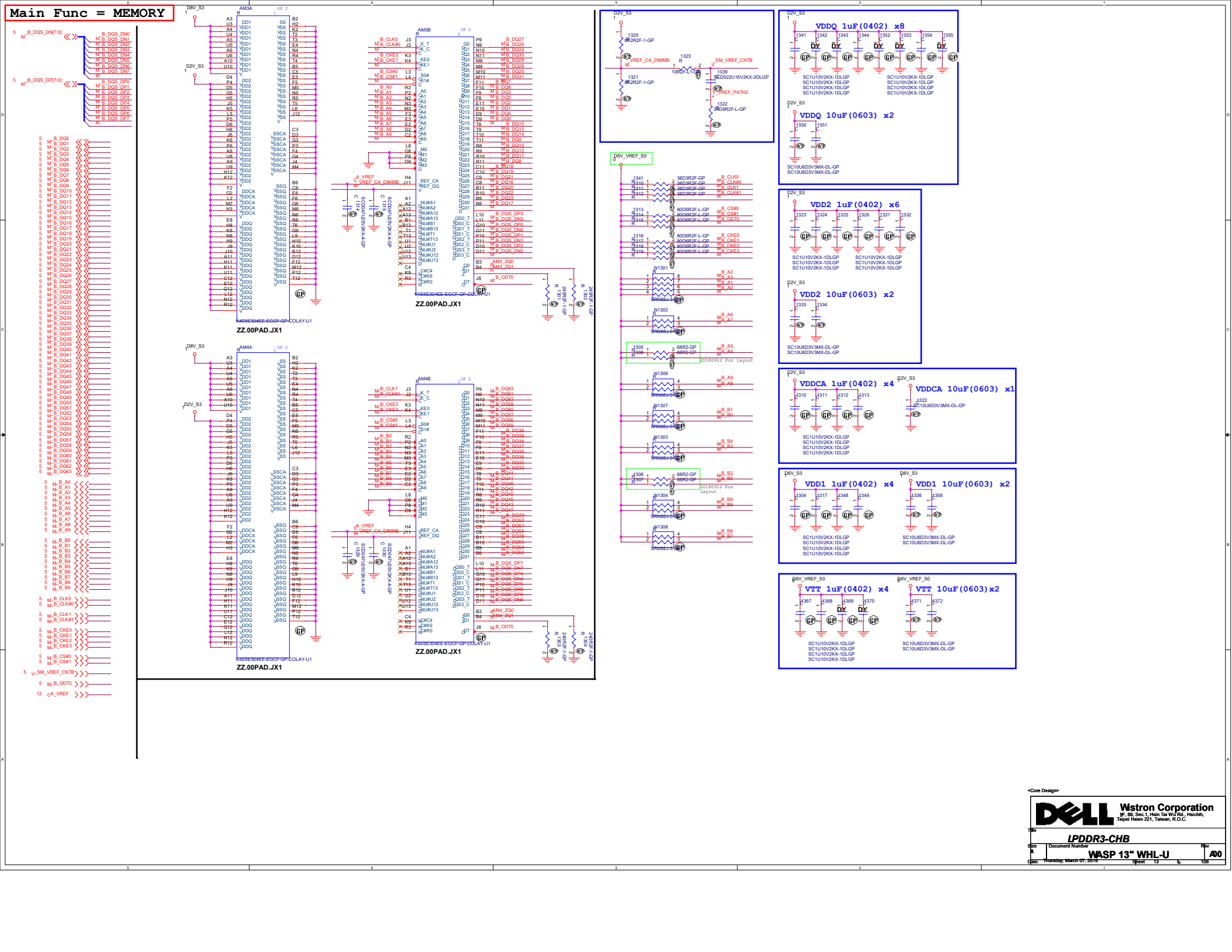

Wistron Corporation
3F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.


Title: LPDDR3-CHA

Size: A | Document Number: WASP 13" WHL-U | Rev: A00

Date: Thursday, March 07, 2019 | Sheet 12 of 108

# Main Func = MEMORY



# (Blanking)

<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

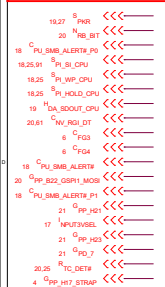
Title: *(Reserved)*

| Size | Document Number | Rev |
|---|---|---|
| A4 | *WASP 13" WHL-U* | *A00* |

Date: Thursday, March 07, 2019 | Sheet 14 of 106

WWW.AliSaler.Com

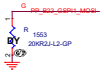
# Main Func = PCH

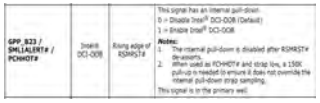


GPP_B14

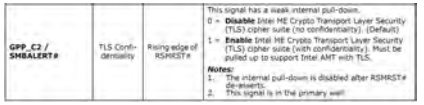
GPP_B18

GPP_B22

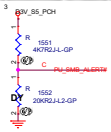


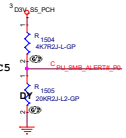
GPP_B23

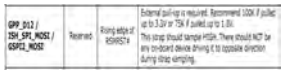


GPP_C2

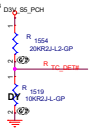


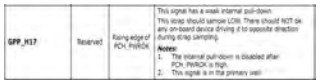
GPP_C5

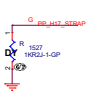


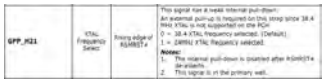



GPP_D12

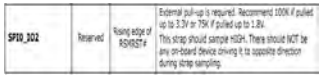


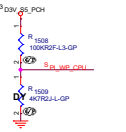


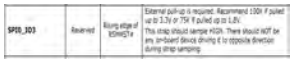



GPP_H21

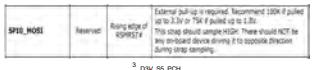


SPI0_IO2

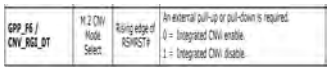


SPI0_IO3

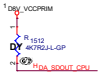


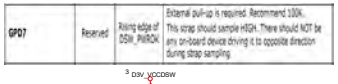
SPI0_MOSI

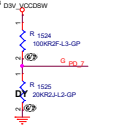


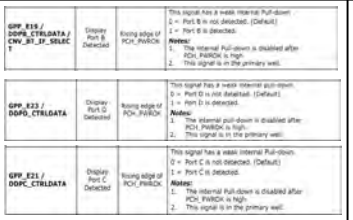
GPP_E2 / CNV_RGI_DT / UART0_TXD

GPP_B2 / HDA_SDO / I2S0_TXD / HDACPU_SDO





(#543016)

| DISPLAY PORT PRESENCE STRAP | |
|---|---|
| CFG[4] | 0 : ENABLED<br>An external Display Port device is connected to the Embedded Display Port. |
| | 1 : DISABLED (Default)<br>No Physical Display Port attached to Embedded DisplayPort*. No connect for disable. |

| [BDW Only]PHYSICAL DEBUG ENABLED (DFX PRIVACY) | |
|---|---|
| CFG[3] | 0 : ENABLED<br>SET DFX ENABLED BIT IN DEBUG INTERFACE MSR |
| | 1 : DISABLED |

PCH strap pin:

<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (Strap pins)

Size: C | Document Number: W ASP 13" WHL-U | Rev: 00

Date: Thursday, March 07, 2019 | Sheet 15 of 106

# Main Func = PCH

## PCIE

61 WLAN_PCIE_RX_N
61 WLAN_PCIE_RX_P
61 WLAN_PCIE_TX_N
61 WLAN_PCIE_TX_P

66 WWAN_PCIE_RX_N11
66 WWAN_PCIE_RX_P11
66 WWAN_PCIE_TX_N11
66 WWAN_PCIE_TX_P11

66 WWAN_PCIE_RX_N12
66 WWAN_PCIE_RX_P12
66 WWAN_PCIE_TX_N12
66 WWAN_PCIE_TX_P12

63 SSD_SATA_RX_N
63 SSD_SATA_RX_P
63 SSD_SATA_TX_N
63 SSD_SATA_TX_P

63 SSD_PCIE_RX_N1
63 SSD_PCIE_RX_P1
63 SSD_PCIE_TX_N1
63 SSD_PCIE_TX_P1

63 SSD_PCIE_RX_N2
63 SSD_PCIE_RX_P2
63 SSD_PCIE_TX_N2
63 SSD_PCIE_TX_P2

63 SSD_PCIE_RX_N3
63 SSD_PCIE_RX_P3
63 SSD_PCIE_TX_N3
63 SSD_PCIE_TX_P3

76 GFX_PCIE_RX_N0
76 GFX_PCIE_RX_P0
76 GFX_PCIE_TX_N0
76 GFX_PCIE_TX_P0

76 GFX_PCIE_RX_N1
76 GFX_PCIE_RX_P1
76 GFX_PCIE_TX_N1
76 GFX_PCIE_TX_P1

76 GFX_PCIE_RX_N2
76 GFX_PCIE_RX_P2
76 GFX_PCIE_TX_N2
76 GFX_PCIE_TX_P2

76 GFX_PCIE_RX_P3
76 GFX_PCIE_RX_N3
76 GFX_PCIE_TX_N3
76 GFX_PCIE_TX_P3

## USB3.0

66 USB1_USB30_RX_N
66 USB1_USB30_RX_P

66 USB1_USB30_TX_N
66 USB1_USB30_TX_P

71 USB4_USB30_RX_N
71 USB4_USB30_RX_P

71 USB4_USB30_TX_N
71 USB4_USB30_TX_P

## USB2.0

72 USB4_USB20_N
72 USB4_USB20_P

66 USB1_USB20_N
66 USB1_USB20_P

55 CCD_USB20_N
55 CCD_USB20_P

61 BT_USB20_N
61 BT_USB20_P

92 FP1_USB20_N
92 FP1_USB20_P

66 WWAN_USB20_N
66 WWAN_USB20_P

66 USB_OC0#
72 USB_OC3#

24 mCARD_PCIE#_SATA

63 SSD_DEVSLP
63 M2_SSD_PEDET

64 PCH_SATA_LED#

66 WSSD_DEVSLP

## GPU

GFX_PCIE_TX_N0 C1606 1 — SCD22U16V2KX-DL-GP — GFX_PCIE_TX_C_N0
GFX_PCIE_TX_P0 C1605 1 — SCD22U16V2KX-DL-GP — GFX_PCIE_TX_C_P0
GFX_PCIE_TX_N1 C1608 1 — SCD22U16V2KX-DL-GP — GFX_PCIE_TX_C_N1
GFX_PCIE_TX_P1 C1607 1 — SCD22U16V2KX-DL-GP — GFX_PCIE_TX_C_P1
GFX_PCIE_TX_N2 C1610 1 — SCD22U16V2KX-DL-GP — GFX_PCIE_TX_C_N2
GFX_PCIE_TX_P2 C1609 1 — SCD22U16V2KX-DL-GP — GFX_PCIE_TX_C_P2
GFX_PCIE_TX_N3 C1612 1 — SCD22U16V2KX-DL-GP — GFX_PCIE_TX_C_N3
GFX_PCIE_TX_P3 C1611 1 — SCD22U16V2KX-DL-GP — GFX_PCIE_TX_C_P3

#543016:
220 nF nominal capacitors are recommended for Gen 3.
100 nF nominal capacitors are recommended for Gen 2.

## WLAN

## 2ND M.2

## SSD

R1604 1 — 2 100R2F-L1-GP-U

## CPU1H

8 OF 20

GFX_PCIE_RX_N0 BW9 — P CIE5_RXN/USB31_5_RXN
GFX_PCIE_RX_P0 BW8 — P CIE5_RXP/USB31_5_RXP
GFX_PCIE_TX_C_N0 BW4 — P CIE5_TXN/USB31_5_TXN
GFX_PCIE_TX_C_P0 BW3 — P CIE5_TXP/USB31_5_TXP
GFX_PCIE_RX_N1 BU6 — P CIE6_RXN/USB31_6_RXN
GFX_PCIE_RX_P1 BU5 — P CIE6_RXP/USB31_6_RXP
GFX_PCIE_TX_C_N1 BU4 — P CIE6_TXN/USB31_6_TXN
GFX_PCIE_TX_C_P1 BU3 — P CIE6_TXP/USB31_6_TXP
GFX_PCIE_RX_N2 BT7 — P CIE7_RXN
GFX_PCIE_RX_P2 BT6 — P CIE7_RXP
GFX_PCIE_TX_C_N2 BU2 — P CIE7_TXN
GFX_PCIE_TX_C_P2 BU1 — P CIE7_TXP
GFX_PCIE_RX_N3 BU9 — P CIE8_RXN
GFX_PCIE_RX_P3 BU8 — P CIE8_RXP
GFX_PCIE_TX_C_N3 BT4 — P CIE8_TXN
GFX_PCIE_TX_C_P3 BT3 — P CIE8_TXP
BP5 — P CIE9_RXN
BP6 — P CIE9_RXP
BR2 — P CIE9_TXN
BR1 — P CIE9_TXP
WLAN_PCIE_RX_N BN6 — P CIE10_RXN
WLAN_PCIE_RX_P BN5 — P CIE10_RXP
WLAN_PCIE_TX_N BR4 — P CIE10_TXN
WLAN_PCIE_TX_P BR3 — P CIE10_TXP
WWAN_PCIE_RX_N11 BN10 — P CIE11_RXN/SATA0_RXN
WWAN_PCIE_RX_P11 BN8 — P CIE11_RXP/SATA0_RXP
WWAN_PCIE_TX_N11 BN4 — P CIE11_TXN/SATA0_TXN
WWAN_PCIE_TX_P11 BN3 — P CIE11_TXP/SATA0_TXP
WWAN_PCIE_RX_N12 BL6 — P CIE12_RXN/SATA1A_RXN
WWAN_PCIE_RX_P12 BL5 — P CIE12_RXP/SATA1A_RXP
WWAN_PCIE_TX_N12 BN2 — P CIE12_TXN/SATA1A_TXN
WWAN_PCIE_TX_P12 BN1 — P CIE12_TXP/SATA1A_TXP
SSD_PCIE_RX_N3 BK6 — P CIE13_RXN
SSD_PCIE_RX_P3 BK5 — P CIE13_RXP
SSD_PCIE_TX_N3 BM4 — P CIE13_TXN
SSD_PCIE_TX_P3 BM3 — P CIE13_TXP
SSD_PCIE_RX_N2 BJ6 — P CIE14_RXN
SSD_PCIE_RX_P2 BJ5 — P CIE14_RXP
SSD_PCIE_TX_N2 BL2 — P CIE14_TXN
SSD_PCIE_TX_P2 BL1 — P CIE14_TXP
SSD_PCIE_RX_N1 BG5 — P CIE15_RXN/SATA1B_RXN
SSD_PCIE_RX_P1 BG6 — P CIE15_RXP/SATA1B_RXP
SSD_PCIE_TX_N1 BL4 — P CIE15_TXN/SATA1B_TXN
SSD_PCIE_TX_P1 BL3 — P CIE15_TXP/SATA1B_TXP
SSD_SATA_RX_N BE5 — P CIE16_RXN/SATA2_RXN
SSD_SATA_RX_P BE6 — P CIE16_RXP/SATA2_RXP
SSD_SATA_TX_N BJ4 — P CIE16_TXN/SATA2_TXN
SSD_SATA_TX_P BJ3 — P CIE16_TXP/SATA2_TXP
PCIE_RCOMPN CE6 — P CIE_RCOMP_N
PCIE_RCOMPP CE5 — P CIE_RCOMP_P
CR28 — G PP_H12/M2_SKT2_CFG0
CP28 — G PP_H13/M2_SKT2_CFG1
CN28 — G PP_H14/M2_SKT2_CFG2
CM28 — G PP_H15/M2_SKT2_CFG3

WHISKEY-LAKE-GP
ZZ.00CPU.271

P CIE1_RXN/USB31_1_RXN — BY8
P CIE1_RXP/USB31_1_RXP — BY9
P CIE1_TXN/USB31_1_TXN — CA2
P CIE1_TXP/USB31_1_TXP — CA1
P CIE2_RXN/USB31_2_RXN/SSIC_1_RXN — BY7
P CIE2_RXP/USB31_2_RXP/SSIC_1_RXP — BY6
P CIE2_TXN/USB31_2_TXN/SSIC_1_TXN — BY4
P CIE2_TXP/USB31_2_TXP/SSIC_1_TXP — BY3
P CIE3_RXN/USB31_3_RXN — BW6
P CIE3_RXP/USB31_3_RXP — BW5
P CIE3_TXN/USB31_3_TXN — BW2
P CIE3_TXP/USB31_3_TXP — BW1
P CIE4_RXN/USB31_4_RXN — CE3
P CIE4_RXP/USB31_4_RXP — CE4
P CIE4_TXN/USB31_4_TXN — CE1
P CIE4_TXP/USB31_4_TXP — CE2
U SB2N_1 — CG3
U SB2P_1 — CG4
U SB2N_2 — CD3
U SB2P_2 — CD4
U SB2N_3 — CG5
U SB2P_3 — CG6
U SB2N_4 — CC1
U SB2P_4 — CC2
U SB2N_5 — CG8
U SB2P_5 — CG9
U SB2N_6 — CB8
U SB2P_6 — CB9
U SB2N_7 — CH5
U SB2P_7 — CH6
U SB2N_8 — CC3
U SB2P_8 — CC4
U SB2N_9 — CC5
U SB2P_9 — CE8
U SB2N_10 — CC6
U SB2P_10 — CK6
U SB2_COMP — CK5
U SB_ID — CK8
U SB_VBUSSENSE — CK9
G PP_E9/USB2_OC0#/GP_BSSB_CLK — CP8
G PP_E10/USB2_OC1#/GP_BSSB_DI — CR8
G PP_E11/USB2_OC2# — CM8
G PP_E12/USB2_OC3# — CN8
G PP_E4/DEVSLP0 — CM10
G PP_E5/DEVSLP1 — CP10
G PP_E6/DEVSLP2 — CN7
G PP_E0/SATAXPCIE0/SATAGP0 — AR3
G PP_E1/SATAXPCIE1/SATAGP1
G PP_E2/SATAXPCIE2/SATAGP2
G PP_E8/SATALED#/SPI1_CS1#
R SVD#AR3

BB1_USB30_RX_N — IO board USB3.1
BB1_USB30_RX_P
BB1_USB30_TX_N
BB1_USB30_TX_P

(#545659)
The xHCI controller supports USB Debug port on all USB3.0 capable ports.

BB4_USB30_RX_N — USB3.1 Type C
BB4_USB30_RX_P
BB4_USB30_TX_N
BB4_USB30_TX_P

USB_USB20_N
USB_USB20_P

BB4_USB20_N — USB3.1 Type C
BB4_USB20_P

BP1_USB20_N — Fingerprint Reader
BP1_USB20_P

BCD_USB20_N — CAMERA
BCD_USB20_P

WWAN_USB20_N
WWAN_USB20_P

BT_USB20_N
BT_USB20_P

USBCOMP
USB2_ID
USB2_VBUSSENSE

USB_OC0#
USB_OC1#
USB_OC2#
USB_OC3#

SIO_EXT_SCI#
VSSD_DEVSLP
SSD_DEVSLP

SSD_M2_SSD_PEDET#
M2_SSD_PEDET

PCH_SATA_LED#

(#543611)
The SATALED# signal is open-collector and requires a weak external pull-up (8.2 kΩ to 10 kΩ) to Vcc3_3.

3D3V_S0
R1606 1 — 2 10KR2J-L-GP — PCH_SATA_LED#
R1608 1 — 2 10KR2J-L-GP — SIO_EXT_SCI#

3D3V_S5_PCH
RN1601
1 — 8 USB_OC3#
2 — 7 USB_OC2#
3 — 6 USB_OC1#
4 — 5 USB_OC0#
SRN10KJ-8-GP

R1601 1 — 2 0R2J-L-GP — USB2_ID
R1602 1 — 2 0R2J-L-GP — USB2_VBUSSENSE
R1603 1 — 2 113R2F-GP — USBCOMP

R1605
2ND_M2_SSD_PEDET# 1 — 2 mCARD_PCIE#_SATA
From EC
0R0402-PAD

(#543016)
Unused SATAGP[2:0]/GPP_E[2:0] pins must be terminated to either 3.3 V rail or GND using 8.2 kΩ to 10 kΩ on the motherboard. Do not use both pull-up and pull-down. Either pull-up or pull-down is acceptable.

(#571021_CFLU) When used as DEVSLP, no external pull-up or pull-down termination required from SATA Host DEVSLP.

**Table 24-3. PCI Express* Link Configurations Supported**

| SKL | PCIe Link Config | PCI Express* Lanes 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| U | 1x4 | Port1 | | | | Port5 | | | | Port9 | | | |
| | 2x2 | Port1 | | Port3 | | Port5 | | Port7 | | Port9 | | Port11 | |
| | 1x2 + 2x1 | Port1 | | Port3 | Port4 | Port5 | | Port7 | Port8 | Port9 | | Port11 | Port12 |
| | 4x1 | Port1 | Port2 | Port3 | Port4 | Port5 | Port6 | Port7 | Port8 | Port9 | Port10 | Port11 | Port12 |
| Y | 1x4 | Port1 | | | | Port5 | | | | | | | |
| | 2x2 | Port1 | | Port3 | | Port5 | | Port7 | | | | | |
| | 1x2 + 2x1 | Port1 | | Port3 | Port4 | Port5 | | Port7 | Port8 | | | | |
| | 4x1 | Port1 | Port2 | Port3 | Port4 | Port5 | Port6 | Port7 | Port8 | | | | |
| | 1x2 | | | | | | | | | Port9 | | | |
| | 2x1 | | | | | | | | | Port9 | Port10 | | |

**Table 24-2. PCI Express* Port Feature Details**

| SKL | Max Device (Ports) | Max Lanes | PCIe* Gen Type | Encoding | Transfer Rate (MT/s) | Theoretical Max Bandwidth (GB/s) x1 | x2 | x4 |
|---|---|---|---|---|---|---|---|---|
| U | 6 | 12 | 1 | 8b/10b | 2500 | 0.25 | 0.50 | 1.00 |
| | | | 2 | 8b/10b | 5000 | 0.50 | 1.00 | 2.00 |
| | | | 3 | 128b/130b | 8000 | 1.00 | 2.00 | 3.94 |
| Y | 5 | 10 | 1 | 8b/10b | 2500 | 0.25 | 0.50 | 1.00 |
| | | | 2 | 8b/10b | 5000 | 0.50 | 1.00 | 2.00 |

**Layout Note:**

1. Trace Width: 4 mils min (breakout) 12-15 mils (trace)
Note: Must maintain low DC resistance routing (<0.1 ohm).
2. Isolation Spacing: At least 12 mils to any adjacent high speed I/O.

<Core Design>

Wistron Corporation
2F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(PCIE/SATA/USB)
Size: B | Document Number: WASP 13" WHL-U | Rev: A00
Date: Thursday, March 07, 2019 | Sheet 16 of 106

WWW.AliSaler.Com

# Main Func = PCH

| | |
|---|---|
| 24 | SYS_PWROK |
| 24,26 | RESET_OUT# |
| 24,40,46 | VCCST_PWRGD |
| 24,64 | PCH_RSMRST# |
| 25,45 | 3V_5V_PWRGD |
| 40,91 | PM_SLP_S0# |
| 40 | PM_SLP_S3# |
| 40,51,92 | PM_SLP_S4# |
| 24 | SIO_PWRBTN# |
| 44 | AC_IN# |
| 15 | INPUT3VSEL |
| 61,63,66,76,91 | PLTRST#_CPU |
| 3 | H_CPUPWRGD |

1D8V_VCCPRIM
R1738 1 DY 2 10KR2J-L-GP ME_SUS_PWR_ACK_R

3D3V_VCCDSW
RN1704 1 4 AC_PRESENT
2 3 PCIE_WAKE#_CPU
SRN10KJ-GP
R1707 1 2 10KR2J-L-GP LAN_WAKE#

RTC_AUX_S5
#544669 (CRB): 330k.
R1730 1 2 330KR2J-L1-GP SM_INTRUDER#

3D3V_VCCPRIM
R1731 1 2 100KR2F-L3-GP EXT_PWR_GATE#
R1701 1 2 10KR2J-L-GP XDP_DBRESET#

3D3V_S5
R1721 1 2 10KR2J-L-GP GPD11/LANPHYPC
R1717 1 2 10KR2J-L-GP SYS_PWROK
RN1703 1 4 PM_RSMRST#
2 3 PM_PCH_PWROK
SRN100KJ-GP

SUSACK#_R R1708 1 DY 2 ME_SUS_PWR_ACK_R
0R2J-2-GP
RESET_OUT# 1 R1706 2 0R0402-PAD PM_PCH_PWROK
PM_RSMRST# 1 R1704 2 0R0402-PAD PCH_DPWROK

CPU1K 11 OF 20

| | | | |
|---|---|---|---|
| PCH_PLTRST# | BJ35 | GPP_B13/PLTRST# | GPP_B12/SLP_S0# BJ37 PM_SLP_S0# |
| XDP_DBRESET# | CN10 | SYS_RESET# | GPD4/SLP_S3# BU36 PM_SLP_S3# |
| PM_RSMRST# | BR36 | RSMRST# | GPD5/SLP_S4# BU27 PM_SLP_S4# |
| | | | GPD10/SLP_S5# BT29 PM_SLP_S5# 1 TP1710 |
| H_CPUPWRGD | AR2 | PROCPWRGD | BU29 |
| VCCST_PWRGD_R | BJ2 | VCCST_PWRGOOD | SLP_SUS# BT31 |
| | | | SLP_LAN# |
| SYS_PWROK | CR10 | SYS_PWROK | GPD9/SPL_WLAN# BT30 AUX_EN_WOWL 1 TP1715 |
| PM_PCH_PWROK | BP31 | PCH_PWROK | GPD6/SLP_A# BU37 PM_SLP_A# 1 TP1706 |
| PCH_DPWROK | BP30 | DSW_PWROK | |
| ME_SUS_PWR_ACK_R | BV34 | GPP_A13/SUSWARN#/SUSPWRDACK | GPD3/PWRBTN# BU28 SIO_PWRBTN# 1 TP1714 |
| SUSACK#_R | BY32 | GPP_A15/SUSACK# | GPD1/ACPRESENT BU35 AC_PRESENT |
| | | | GPD0/BATLOW# BV36 PCH_BATLOW# |
| PCIE_WAKE#_CPU | BU30 | WAKE# | |
| LAN_WAKE# | BU32 | GPD2/LAN_WAKE# | INTRUDER# BR35 SM_INTRUDER# |
| GPD11/LANPHYPC | BU34 | GPD11/LANPHYPC | |
| | | | GPP_B11/EXT_PWR_GATE# CC37 EXT_PWR_GATE# |
| | | | GPP_B2/VRALERT# CC36 VRALERT# 1 TP1708 |
| | | | INPUT3VSEL BT27 INPUT3VSEL |

WHISKEY-LAKE-GP
ZZ.00CPU.271

B ATLOW#:
Pull-up required even if not implemented.

20180905
EMC add

SYS_PWROK — AZ5725-01FDR7G-GP ED1701
PLTRST#_CPU — AZ5725-01FDR7G-GP ED1702
RESET_OUT# — TVL5VB1-DFN1006-2L-GP ED1703
3V_5V_PWRGD — TVL5VB1-DFN1006-2L-GP ED1704

3D3V_AUX_S5
R1727 1 2 100KR2J-1-GP
R1726 10KR2J-L-GP
Q1701
PM_RSMRST# R1702 1 2 PCH_RSMRST#
1KR2J-1-GP
3V_5V_POK# 3V_5V_PWRGD
PJT138KA-GP
075.00138.0A7C

3D3V_VCCDSW
R1722 10KR2J-L-GP
PCH_BATLOW#
R1723 DY 10KR2J-L-GP

Reserve by NON DS3 function 20150413
D1701 RB520S30-GP
A K AC_IN#
83.R2003.A8M
Q1702
3D3V_AUX_S5
R1737 1 2 100KR2J-1-GP PM_RSMRST#_M
AC_PRESENT
PM_RSMRST#
2N7002KDW-1-GP
75.27002.F7C

PM_RSMRST# — AZ5725-01FDR7G-GP ED1706
VCCST_PWRGD_R — AZ5725-01FDR7G-GP ED1707
20180918
EMC Modify

3D3V_S0
R1718 DY 100KR2F-L3-GP
R1716 100KR2F-L3-GP
VCCST_PWRGD 1 2 VCCST_PWRGD_R
R1719 47KR2F-GP
DY C1711 SCD1U16V2KX-3DLGP

#543016 Rev0.7
1. VCCST_PWRGD is only 1.0 V tolerant.
2. VCCST_PWRGD must go low during Sx pwr states, regardless of the voltage level of VCCST

PLTRST#_CPU 1 R1713 2 PCH_PLTRST#
0R0402-PAD
R1715 100KR2J-1-GP
DY C1701 SC220P50V2KX-3DLGP

(PDG#543016)
WAKE#: Ensure that WAKE# signal Trise (Maximum) is <100 ns.

<Core Design>

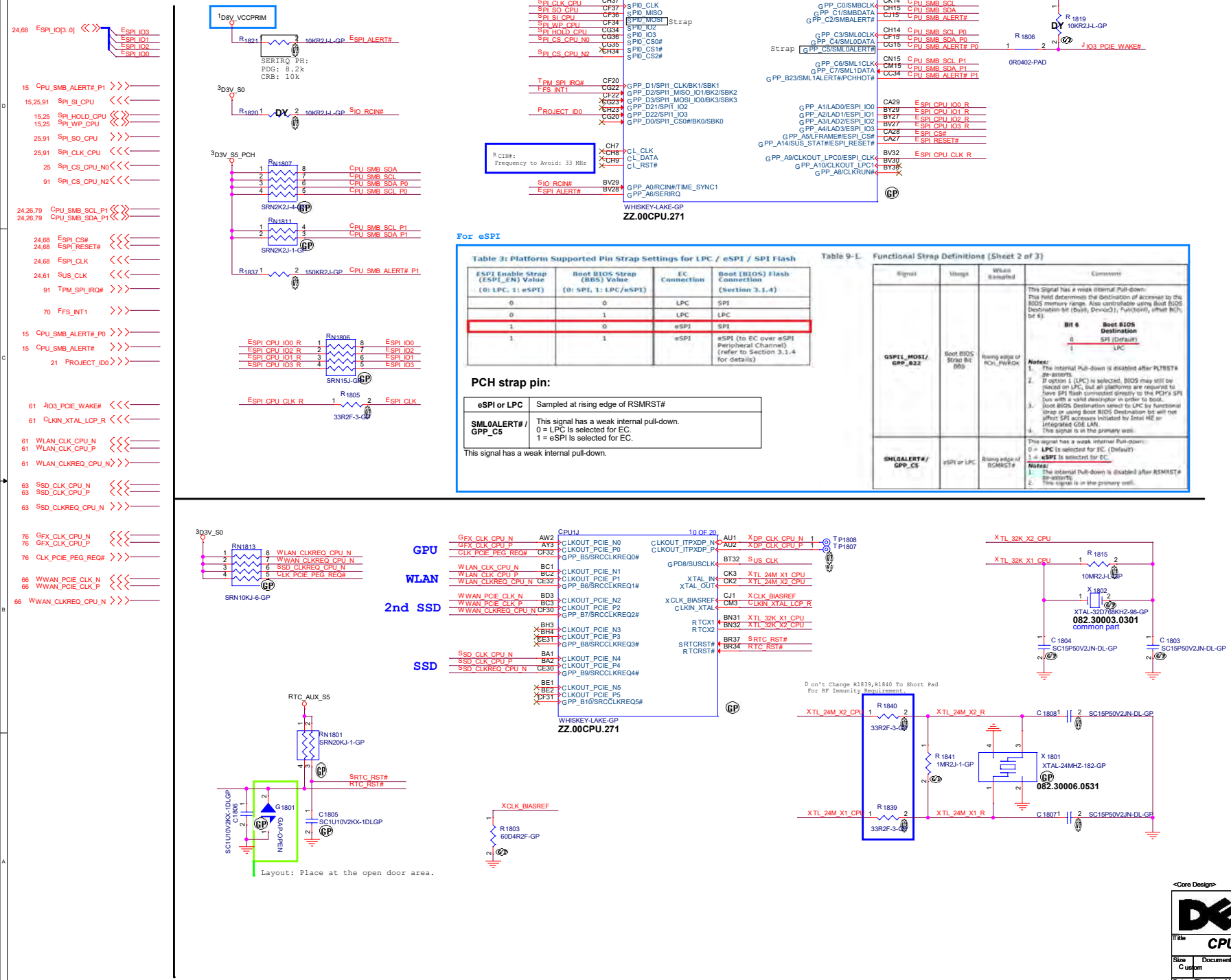
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(POWER MANAGEMENT)

| Size | Document Number | Rev |
|---|---|---|
| Custom | WASP 13" WHL-U | A 00 |

Date: Thursday, March 07, 2019 Sheet 17 of 106

# Main Func = PCH





<Core Design>
Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.


Title: CPU(SPI/ESPI/SMBS/XTAL/CLK)

Size: C Custom | Document Number: WASP 13" WHL-U | Rev: A00

Date: Thursday, March 07, 2019 | Sheet 18 of 106

WWW.AliSaler.Com

# Main Func = PCH

27 HDA_SDIN0_CPU
27 HDA_SYNC_CODEC
27 HDA_BITCLK_CODEC
27 HDA_SDOUT_CODEC

55 DMIC_SCL_CPU
55 DMIC_SDA_CPU

61 BT_PCMFRM_RSTN
61 BT_PCMOUT_CLKREQ0
65 KB_LED_BL_DET
24,85 DGPU_PWROK
15,27 SPKR
98 ME_FWP_SW
15 HDA_SDOUT_CPU

33 SD_PWR_EN#

33 SD_SDATA0
33 SD_SDATA1
33 SD_SDATA2
33 SD_SDATA3

33 SD_CLK
33 SD_CMD

33 SD_CD_N
33 SD_WP

CPU1G — 7 OF 20

HDA_SYNC_CPU BN34 — HDA_SYNC/I2S0_SFRM
HDA_BITCLK_CPU BN37 — HDA_BCLK/I2S0_SCLK
HDA_SDOUT_CPU BN36 — HDA_SDO/I2S0_TXD
HDA_SDIN0_CPU BN35 — HDA_SDI0/I2S0_RXD
BL36 — HDA_SDI1/I2S1_RXD/SNDW1_DATA
TP1903 TPAD14-OP-GP 1 HDA_RST_N_CPU BL35 — HDA_RST#/I2S1_SCLK/SNDW1_CLK
KB_LED_BL_DET CK23 — GPP_D23/I2S_MCLK
BL37 — I2S1_SFRM/SNDW2_CLK
BL34 — I2S1_TXD/SNDW2_DATA

GPP_H1_SFRM CJ32 — GPP_H1/I2S2_SFRM/CNV_BT_I2S_BCLK/CNV_RF_RESET#
CH32 — GPP_H0/I2S2_SCLK/CNV_BT_I2S_SCLK
GPP_H2_CLKREQ0 CH29 — GPP_H2/I2S2_TXD/CNV_BT_I2S_SDI/MODEM_CLKREQ
CH30 — GPP_H3/I2S2_RXD/CNV_BT_I2S_SDO
GPP_A17/SD_VDD1_PWR_EN#/ISH_GP7
DMIC_SCL_CPU CP24 — GPP_D19/DMIC_CLK0/SNDW4_CLK
DMIC_SDA_CPU CN24 — GPP_D20/DMIC_DATA0/SNDW4_DATA
GPP_A16/SD_1P8_SEL
TPM_ID CK25 — GPP_D17/DMIC_CLK1/SNDW3_CLK
DGPU_PWROK CJ25 — GPP_D18/DMIC_DATA1/SNDW3_DATA
SD_1P8_RCOMP
SD_3P3_RCOMP
SPKR CF35 — GPP_B14/SPKR

GPP_G0/SD_CMD CH36 SD_CMD
GPP_G1/SD_DATA0 CL35 SD_SDATA0
GPP_G2/SD_DATA1 CL36 SD_SDATA1
GPP_G3/SD_DATA2 CM35 SD_SDATA2
GPP_G4/SD_DATA3 CN35 SD_SDATA3
GPP_G5/SD_CD# CH35 SD_CD_N
GPP_G6/SD_CLK CK36 SD_CLK
GPP_G7/SD_WP CK34 SD_WP

BW36 SD_PWR_EN#
BY31
CK33 SD_RCOMP — R 19011 200R2F-L-GP — 2
CM34

GP

WHISKEY-LAKE-GP
**ZZ.00CPU.271**

3D3V_S5
R1910 10KR2J-L-GP
fTPM
TPM_ID
R1911 10KR2J-L-GP
TPM

HDA_SYNC_CODEC — R 19081 — 0R2J-L-GP — HDA_SYNC_CPU

**Layout Note:** R1920 & R1921 need to close for merge prepare

HDA_BITCLK_CODEC — R 19201 — 0R2J-L-GP — HDA_BITCLK_CPU
HDA_SDOUT_CODEC — R 19211 — 33R2F-3-GP — HDA_SDOUT_CPU

ME_FWP_SW — R 19091 — 1KR2J-1-GP

BT_PCMFRM_RSTN — R 19131 — 33R2F-3-GP — GPP_H1_SFRM
BT_PCMOUT_CLKREQ0 — R 19121 — 33R2F-3-GP — GPP_H2_CLKREQ0

HDA_BITCLK_CODEC
DY E C1901 SC10P50V2JN-4DLGP
20180904 EMC add

## Strap pin:

| | |
|---|---|
| **Port B / Port C Detected** | Sampled at rising edge of PCH_PWROK |
| **DDPB_CTRLDATA** | 0 = Port B is not detected.<br>* 1 = Port B is detected. |
| **DDPC_CTRLDATA** | 0 = Port C is not detected.<br>* 1 = Port C is detected. |

These two signals have weak internal pull-down.

<Core Design>

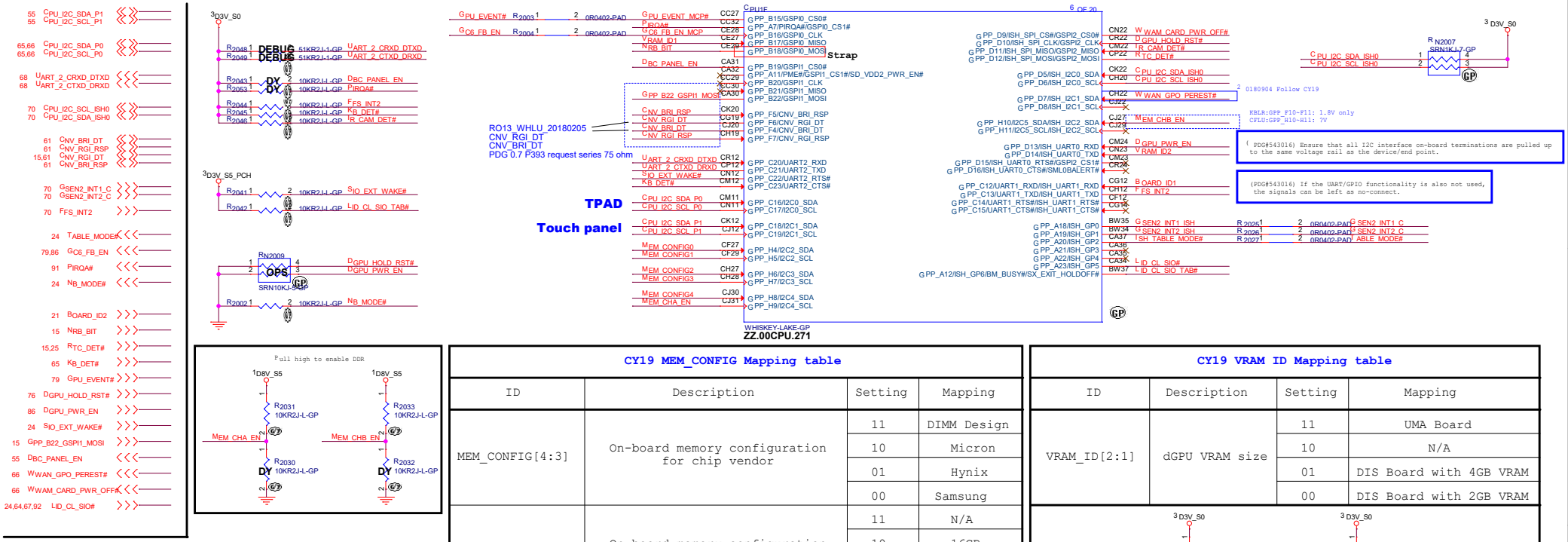
**Wistron Corporation**
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (HDA/I2S/SD/DMIC)**

| Size | Document Number | Rev |
|---|---|---|
| A4 | WASP 13" WHL-U | A00 |

Date: Thursday, March 07, 2019 Sheet 19 of 106

# Main Func = PCH

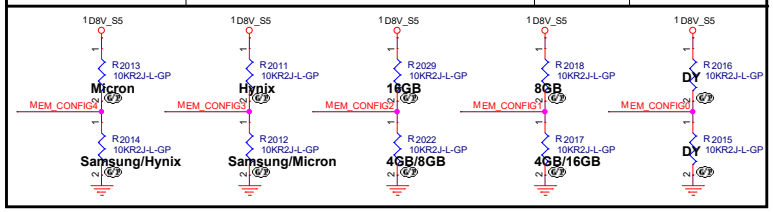






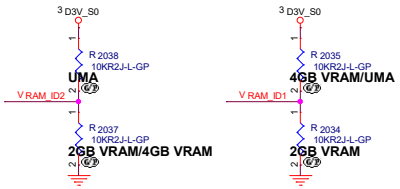
## CY19 MEM_CONFIG Mapping table

| ID | Description | Setting | Mapping |
|---|---|---|---|
| MEM_CONFIG[4:3] | On-board memory configuration for chip vendor | 11 | DIMM Design |
| | | 10 | Micron |
| | | 01 | Hynix |
| | | 00 | Samsung |
| MEM_CONFIG[2:1] | On-board memory configuration for total memory size per channel | 11 | N/A |
| | | 10 | 16GB |
| | | 01 | 8GB |
| | | 00 | 4GB |
| MEM_CONFIG[0] | SDP/DDP Configuration | 1 | SDP |
| | | 0 | DDP |



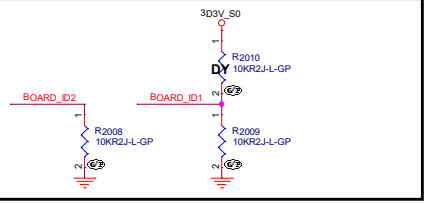

## CY19 VRAM ID Mapping table

| ID | Description | Setting | Mapping |
|---|---|---|---|
| VRAM_ID[2:1] | dGPU VRAM size | 11 | UMA Board |
| | | 10 | N/A |
| | | 01 | DIS Board with 4GB VRAM |
| | | 00 | DIS Board with 2GB VRAM |




## CY19 Board ID Mapping table

| ID | Description | Setting | Mapping |
|---|---|---|---|
| Board ID[2:1] | Board SKU ID | 11 | KBL-U |
| | | 10 | KBL-R |
| | | 01 | N/A |
| | | 00 | SKL-U |





<Core Design>
Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.


Title: CPU_(LPSS/ISH)

| Size | Document Number | Rev |
|---|---|---|
| C ustom | WASP 13" WHL-U | A00 |

Date: Thursday, March 07, 2019 Sheet 20 of 106

WWW.AliSaler.Com

# Main Func = PCH

15 GPD_7
15 GPP_H21
15 GPP_H23
18 PROJECT_ID0
20 BOARD_ID2
40 GPPC_H18_VCCIO_LPM
55 TOUCH_DETECT
21,61 CNV_WR_CLK_DP
21,61 CNV_WR_CLK_DN
21,61 CNV_WR_CLK_DP
21,61 CNV_WR_CLK_DN
61 CNV_WR_DP0
61 CNV_WR_DN0
61 CNV_WR_DP1
61 CNV_WR_DN1
61 WIFI_RF_EN
61 BLUETOOTH_EN
61 CNV_WT_CLK_DP
61 CNV_WT_CLK_DN
61 CNV_WT_DP0
61 CNV_WT_DN0
61 CNV_WT_DP1
61 CNV_WT_DN1
66 WWAN_BB_RST#

3D3V_S0

R2110 1 DY 2 10KR2J-L-GP SPK_ID
R2101 1 2 150R2F-1-GP CNV_WT_RCOMP
R2108 1 2 200R2F-L-GP EMMC_RCOMP

TOUCH_DETECT 1 R2102 2 TOUCH_DETECT_R
0R0402-PAD

GPPC_H18_BOOTMPC 1 R2119 2 GPPC_H18_VCCIO_LPM
0R0402-PAD

R2120 1 DY 2 75KR2J-GP WWAN_BB_RST#

CPU1I 9 OF 20

CNV_WR_DN0 CR30
CNV_WR_DP0 CP30
CNV_WR_DN1 CM30
CNV_WR_DP1 CN30
CNV_WT_DN0 CN32
CNV_WT_DP0 CM32
CNV_WT_DN1 CP33
CNV_WT_DP1 CN33
CNV_WR_CLK_DN CN31
CNV_WR_CLK_DP CP31
CNV_WT_CLK_DN CP34
CNV_WT_CLK_DP CN34
CNV_WT_RCOMP CP32
CR32
CP20
PROJECT_ID1 CK19
PROJECT_ID2 CG17
SPK_ID CR14
BLUETOOTH_EN CP14
TOUCH_DETECT_R CN14
BOARD_ID2 CM14
CJ17
CH17
WWAN_BB_RST# CF17

CNV_WR_D0N
CNV_WR_D0P
CNV_WR_D1N
CNV_WR_D1P
CNV_WT_D0N
CNV_WT_D0P
CNV_WT_D1N
CNV_WT_D1P
CNV_WR_CLKN
CNV_WR_CLKP
CNV_WT_CLKN
CNV_WT_CLKP
CNV_WT_RCOMP#CP32
CNV_WT_RCOMP#CR32
GPP_F0/CNV_PA_BLANKING
GPP_F1
GPP_F2
GPP_C8/UART0_RXD
GPP_C9/UART0_TXD
GPP_C10/UART0_RTS#
GPP_C11/UART0_CTS#
GPP_F8/CNV_MFUART2_RXD
GPP_F9/CNV_MFUART2_TXD
GPP_F23/A4WP_PRESENT

GPP_H18/CPU_C10_GATE# CN27 GPPC_H18_BOOTMPC
GPP_H19/TIMESYNC0 CM27
GPP_H21 CF25 GPP_H21
GPP_H22 CN26
GPP_H23 CM26 GPP_H23
GPP_F10 CK17
GPD7 BV35 GPD_7
GPP_F3 CN20 PROJECT_ID3
GPP_D4/IMGCLKOUT0/BK4/SBK4 CG25 WIFI_RF_EN
GPP_H20/IMGCLKOUT1 CH25

GPP_F12/EMMC_DATA0 CR20
GPP_F13/EMMC_DATA1 CM20
GPP_F14/EMMC_DATA2 CN19
GPP_F15/EMMC_DATA3 CM19
GPP_F16/EMMC_DATA4 CN18
GPP_F17/EMMC_DATA5 CR18
GPP_F18/EMMC_DATA6 CP18
GPP_F19/EMMC_DATA7 CM18
GPP_F20/EMMC_RCLK CM16
GPP_F21/EMMC_CLK CP16
GPP_F11/EMMC_CMD CR16
GPP_F22/EMMC_RESET# CN16

GPP_F:
VCCPGPPF = 1.8V Only

EMMC_RCOMP CK15 EMMC_RCOMP

WHISKEY-LAKE-GP
ZZ.00CPU.271

## PROJECT_ID[1:0]

1D8V_VCCPRIM
R2111 10KR2J-L-GP PROJECT_ID1
R2112 DY 10KR2J-L-GP
1D8V_VCCPRIM
R2113 DY 10KR2J-L-GP PROJECT_ID0
R2114 10KR2J-L-GP

## PROJECT_ID[3:2]

1D8V_VCCPRIM
R2117 10KR2J-L-GP
Inspiron/Vostro
PROJECT_ID3
R2118 10KR2J-L-GP
Latitude
1D8V_VCCPRIM
R2115 10KR2J-L-GP
Inspiron/Latitude
PROJECT_ID2
R2116 10KR2J-L-GP
Vostro

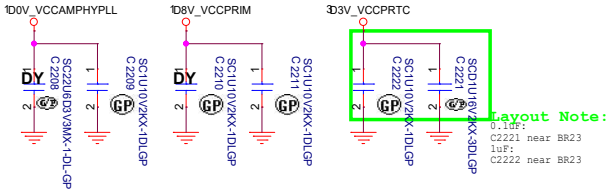
| ID | Description | Setting | Mapping |
|---|---|---|---|
| PROJECT_ID[3:2] | Project Type | 11 | Inspiron |
| | | 10 | Vostro |
| | | 01 | Latitude Reseved |
| | | 00 | N/A |
| PROJECT_ID[1:0] | Project Series | 11 | 3000 Sereis |
| | | 10 | 5000 Sereis |
| | | 01 | 7000 Sereis |
| | | 00 | N/A |

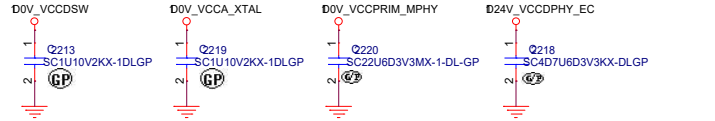
<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

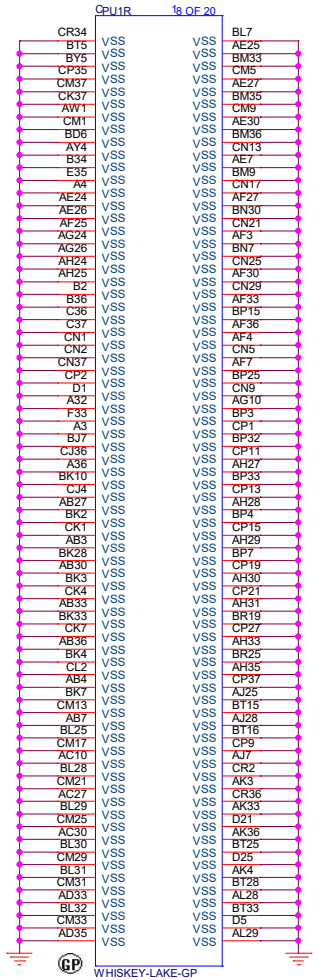
Title: CPU_(POWER1)
Size: A4
Document Number: WASP 13" WHL-U
Rev: A00
Date: Thursday, March 07, 2019
Sheet 21 of 106

# Main Func = PCH

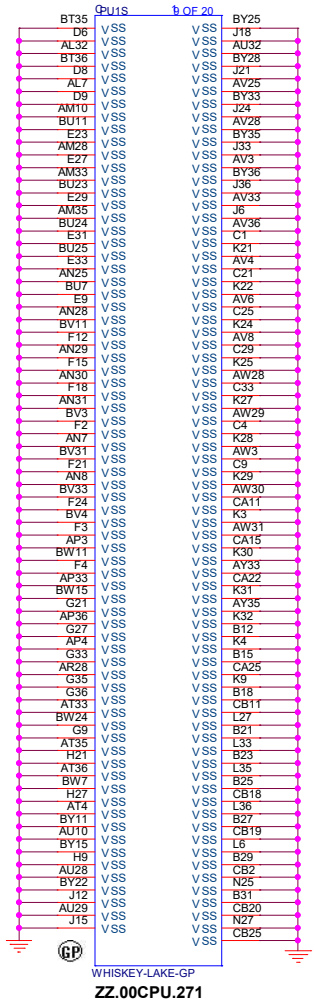


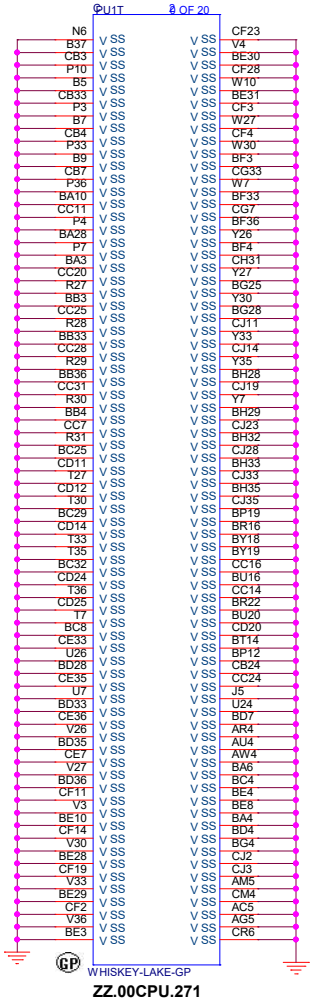
# Main Func = PCH




ZZ.00CPU.271




ZZ.00CPU.271




ZZ.00CPU.271

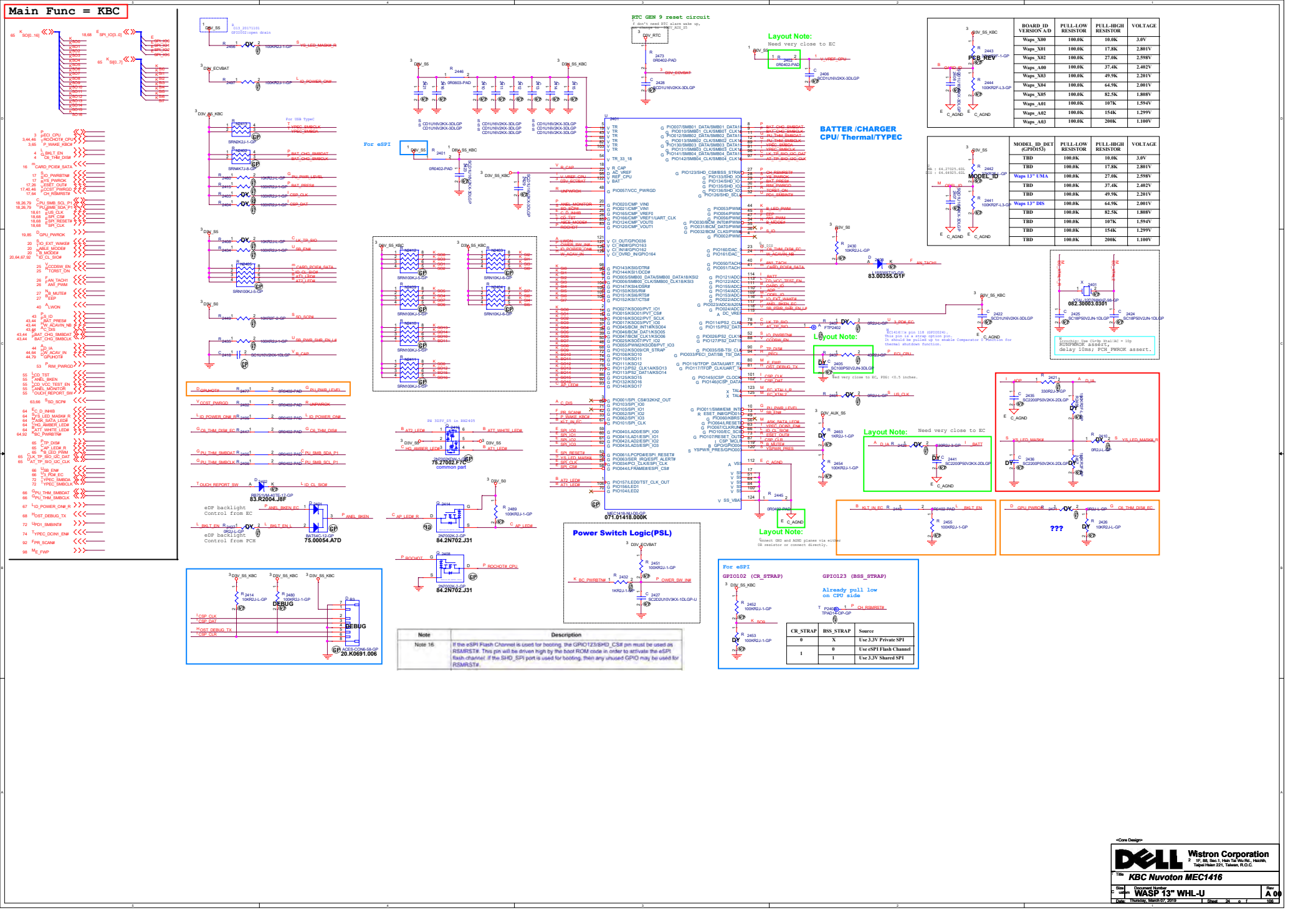
<Core Design>

Wistron Corporation
2F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(VSS)

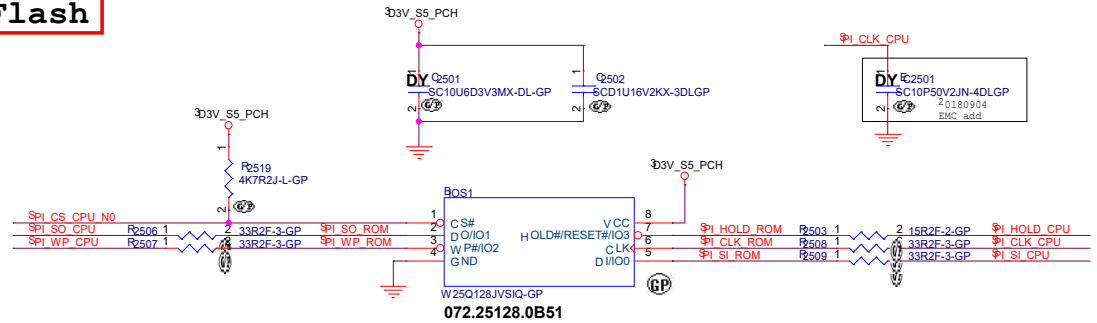
Size: B | Document Number: WASP 13" WHL-U | Rev: A00

Date: Thursday, March 07, 2019 | Sheet 23 of 106


Main Func = KBC
RTC GEN 9 reset circuit
Layout Note:
Need very close to EC
PCB_REV
MODEL_ID
BATTER /CHARGER
CPU/ Thermal/TYPEC
For eSPI
Power Switch Logic(PSL)
Layout Note:
Need very close to EC
Layout Note:
Need very close to EC
Layout Note:
Need very close to EC

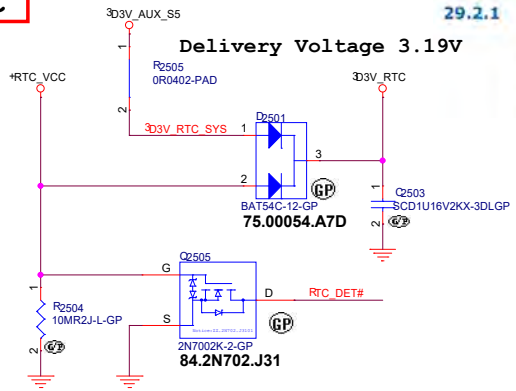
# Main Func = SPI Flash

15,18 SPI_WP_CPU
15,18 SPI_HOLD_CPU
18 SPI_CS_CPU_N0
18,91 SPI_CLK_CPU
15,18,91 SPI_SI_CPU
18,91 SPI_SO_CPU



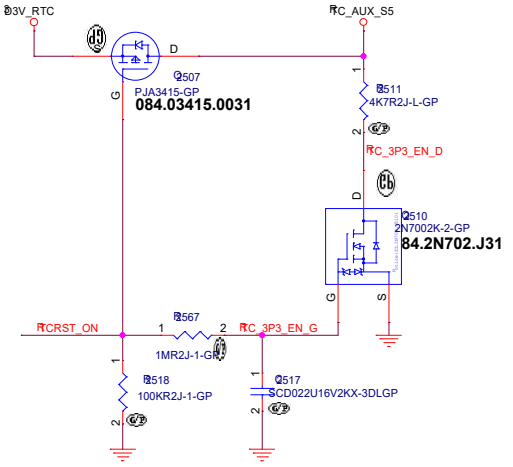

# Main Func = RTC

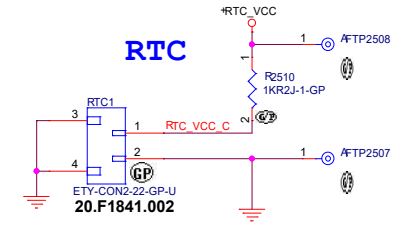
24 RTCRST_ON
24 VCCDSW_EN
17,45 3V_5V_PWRGD
52,53 3V_5V_DSW_OK
15,20 RTC_DET#

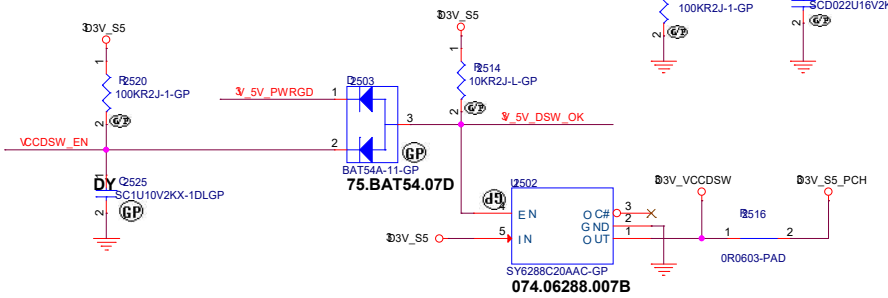



## 29.2.1 VCCRTC External Circuit

On KBL, the VCCRTC max voltage is being reduced to minimize leakage on the ESD diodes and prevent RTC oscillator problems. Whether VCCRTC is sourced from Vbatt in G3 or VCCDSW_3p3 in Non-G3 state, platform designers must ensure the effective voltage at VCCRTC does not exceed 3.2V. The following sections will detail various options platform designers can use to achieve this new specification.




<Core Design>

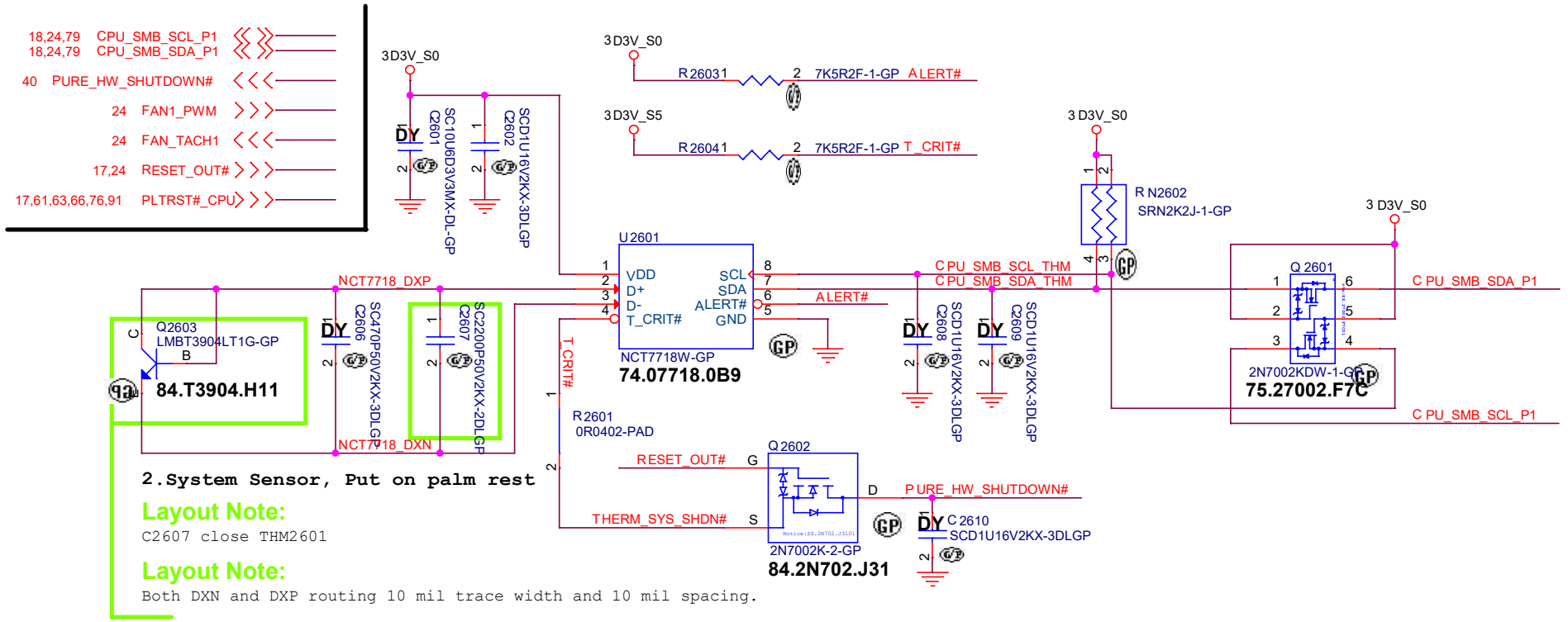
Wistron Corporation
2F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash/RTC

| Size | Document Number | Rev |
|---|---|---|
| B | WASP 13" WHL-U | A00 |

Date: Thursday, March 07, 2019 Sheet 25 of 106

# Main Func = Thermal Sensor




2.System Sensor, Put on palm rest

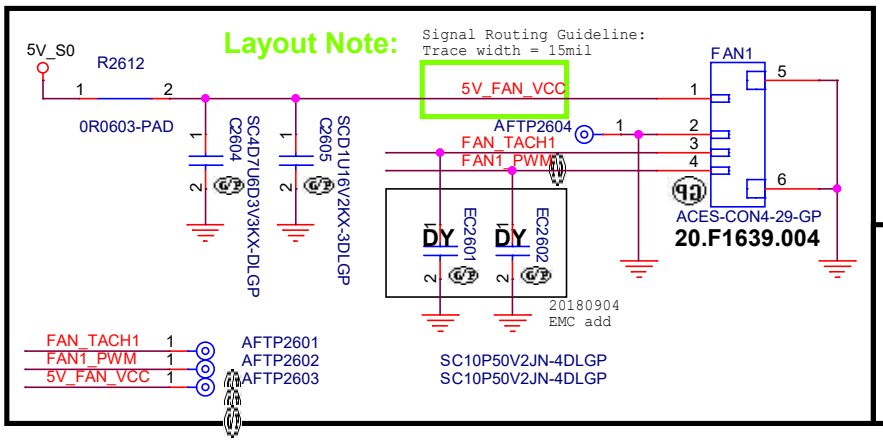
**Layout Note:**

C2607 close THM2601

**Layout Note:**

Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

## PWM FAN1




| TEMPERATURE (℃) | | T_CRIT# | | | | |
|---|---|---|---|---|---|---|
| | | 2KΩ | 7.5KΩ | 10.5KΩ | 14KΩ | 18.7KΩ |
| ALERT# | 2KΩ | 77 | 87 | 97 | 107 | 117 |
| | 7.5KΩ | 79 | 89 | 99 | 109 | 119 |
| | 10.5KΩ | 81 | 91 | 101 | 111 | 121 |
| | 14KΩ | 83 | 93 | 103 | 113 | 123 |
| | 18.7KΩ | 85 | 95 | 105 | 115 | 125 |

**KBC T8**

<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: THERMAL NCT7718W/Fan

| Size | Document Number | Rev |
|---|---|---|
| A 4 | WASP 13" WHL-U | A00 |

Date: Thursday, March 07, 2019 Sheet 26 of 106

WWW.AliSaler.Com

# Audio Codec Chip ALC3204

**Main Func = Audio**

19 HDA_SDIN0_CPU
19 HDA_SDOUT_CODEC
19 HDA_SYNC_CODEC
19 HDA_BITCLK_CODEC

29 AUD_SPK_R+
29 AUD_SPK_R-
29 AUD_SPK_L+
29 AUD_SPK_L-

55 DMIC_SCL_CODEC
55 DMIC_SDA_CODEC

17,40 PM_SLP_S3#
29,66 AUD_SENSE
24 NB_MUTE#
15,19 SPKR
24 BEEP
29,66 AUD_RING
29,66 AUD_SLEEVE

29 LINE1_L
29 LINE1_R

29 LINE1_VREFO
29 MIC2_VREFO_R

29,66 AUD_HP1_JACK_L
29,66 AUD_HP1_JACK_R

5V_S0 — R2701 0R0805-PAD — +5V_PVDD
R2707 0R0805-PAD

1D8V_S0 — R2709 0R0402-PAD — 1D8V_CPVDD

moat

Analog
Digital

1.8V power rail should be supplied by linear regulator, not switching regulator.if switch regulator is unavailable, please make sure that switch frequency operates at out-band(over 20KHz)

1D8V_S0 — R2719 0R0402-PAD — C2710 SC10U6D3V3MX-DL-GP — AUD_AGND

+5V_PVDD >2A

C2713 SC10U6D3V3MX-DL-GP
C2714 SCD1U16V2KX-3DLGP
C2717 SC10U6D3V3MX-DL-GP
C2718 SCD1U16V2KX-3DLGP

Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power

AUD_SPK_L+
AUD_SPK_L-
AUD_SPK_R-
AUD_SPK_R+

DVDD must >= DVDD_IO

3D3V_S0 — R2715 0R0603-PAD — +3V_1D8V_DVDD
C2740 SC22D2U10V3KX-1DLGP
C2741 SCD1U16V2KX-3DLGP

SPKR — R2741 0R0402-PAD — HDA_SPKR_R — D2703 BAT54C-12-GP — AUD_PC_BEEP_C — C2735 SCD1U16V2KX-3DLGP — AUD_PC_BEEP
BEEP — R2734 0R0402-PAD — KBC_BEEP_R
75.00054.A7D
R2735 1KR2J-1-GP
C2739 SC100P50V2JN-3DLGP

Open drain output, pull up to DVDD or max. 5V
For RTC Gen9 reset circuit change power rail. 20170921

3D3V_RTC — R2708 0R0402-PAD — V3D3_STB
3D3V_S0 — R2716 100KR2J-1-GP — DY — DVSS

HDA_SDIN0_CPU — R2724 22R2J-L1-GP — HDA_CODEC_SDIN0
HDA_BITCLK_CODEC — R2723 22R2J-L1-GP — HDA_BITCLK_CODEC_R

AUD_HP1_JACK_L
AUD_HP1_JACK_R

1D8V_CPVDD
C2705 SC22D2U10V3KX-1DLGP-U
C2704 SCD1U16V2KX-3DLGP
C2708 SC22D2U10V3KX-1DLGP-U
C2709 SCD1U16V2KX-3DLGP

U2701 ALC3204-CG-GR-U

| | | | |
|---|---|---|---|
| 30 | CBP | 31 | AVSS2 |
| 29 | CPVDD | 32 | LDO2-CAP |
| 28 | CBN | 33 | AVDD2 |
| 27 | CPVEE | 34 | PVDD1 |
| 26 | HP-OUT-R | 35 | SPK-L+ |
| 25 | HP-OUT-L | 36 | SPK-L- |
| 24 | LINE1-VREFO-L | 37 | SPK-R- |
| 23 | MIC2-VREFO | 38 | SPK-R+ |
| 22 | VREF | 39 | PVDD2 |
| 21 | LDO1-CAP | 40 | PDB |
| | | 41 | GND |

C2711 SC10U6D3V3MX-DL-GP — LDO2_CAP — +3V_1D8V_AVDD
PDB_R

ALC3204
QFN40 (5X5)
071.03204.0003

| | | | |
|---|---|---|---|
| 1 | DVDD | 20 | AVDD1 |
| 2 | GPIO0/DMIC-DATA12 | 19 | AVSS1 |
| 3 | GPIO1/DMIC-CLK | 18 | LINE1-L |
| 4 | SDATA-OUT | 17 | LINE1-R |
| 5 | BIT-CLK | 16 | V D33STB |
| 6 | LDO3-CAP | 15 | MIC2-CAP |
| 7 | SDATA-IN | 14 | LEEV/MIC2-R |
| 8 | DVDD-IO | 13 | RING2/MIC2-L |
| 9 | SYNC | 12 | HP/LINE1-JD_JD1 |
| 10 | DC_DET | 11 | PCBEEP |

C2715 SC10U6D3V3MX-DL-GP

DMIC_SDA_CODEC
DMIC_SCL_CODEC
HDA_SDOUT_CODEC
HDA_BITCLK_CODEC_R
LDO3_CAP
HDA_CODEC_SDIN0
HDA_SYNC_CODEC
DVSS

C2720 SC10U6D3V3MX-DL-GP
C2721 SCD1U16V2KX-3DLGP
C2722 SC10U6D3V3MX-DL-GP
C2723 SC4D7U6D3V3KX-DLGP

place close to pin1
place close to pin8

Analog
Digital
moat

5V_AVDD — R2703 0R0603-PAD — 5V_S0
C2707 SC10U6D3V3MX-DL-GP
C2706 SCD1U16V2KX-3DLGP

Layout Note:
Place close to Pin 20

AUD_AGND
Q2702 SC2D2U10V3KX-1DLGP-U
R2702 100KR2J-1-GP
C2703 SC22D2U10V3KX-1DLGP-U

Azalia I/F EMI

HDA_SDOUT_CODEC — EC2707 SC22P50V2JN-9-GP — DY
HDA_BITCLK_CODEC — EC2711 SC22P50V2JN-9-GP — DY
DMIC_SDA_CODEC — EC2710 SC22P50V2JN-9-GP — DY
DMIC_SCL_CODEC — EC2706 SC33P50V2JN-3DLGP — DY
20180911 Vendor add

6V_1D8V_DVDD — R2717 100KR2J-1-GP — 20180911 Vendor stuff — R2712 0R0402-PAD — NB_MUTE# — RDB_R

6V_1D8V_DVDD — R2710 100KR2J-1-GP — R2711 200KR2F-L-GP — AUD_SENSE — AUD_HPJD_N

moat
20180904 EMC modify

EC2701 SC1KP50V2KX-1DLGP
EC2702 SC1KP50V2KX-1DLGP
EC2703 SC1KP50V2KX-1DLGP
EC2704 SC1KP50V2KX-1DLGP
EC2705 SC1KP50V2KX-1DLGP

R2704 0R0603-PAD
R2705 0R0603-PAD
R2706 0R0603-PAD

Layout Note:
Tied at point only under Codec or near the Codec

<Core Design>

Wistron Corporation
2F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Codec ALC3204
Size: B | Document Number: WASP 13" WHL-U | Rev: A00
Date: Thursday, March 07, 2019 | Sheet 27 of 106

(Blanking)

<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)*

| Size | Document Number | Rev |
|---|---|---|
| A 4 | *WASP 13" WHL-U* | *A 00* |

Date: Thursday, March 07, 2019 | Sheet 28 of 106

WWW.AliSaler.Com

# Main Func = Audio

## Speaker

**Layout Note:**

Speaker trace width >40mil @ 2W4ohm speaker power

27 AUD_SPK_R+
27 AUD_SPK_R-
27 AUD_SPK_L-
27 AUD_SPK_L+

AUD_SPK_R+ ER2901 1 2 0R3J-0-U-GP AUD_SPK_R+_C
AUD_SPK_R- ER2902 1 2 0R3J-0-U-GP AUD_SPK_R-_C
AUD_SPK_L+ ER2903 1 2 0R3J-0-U-GP AUD_SPK_L+_C
AUD_SPK_L- ER2904 1 2 0R3J-0-U-GP AUD_SPK_L-_C

SPK1
ACES-CON4-29-GP
20.F1639.004

| CONN Pin | Net name |
|---|---|
| Pin1 | SPK_L+ |
| Pin2 | SPK_L- |
| Pin3 | SPK_R+ |
| Pin4 | SPK_R- |

C2902 C2901 C2903 C2904
SC1KP50V2KX-1DLGP
SC1KP50V2KX-1DLGP
SC1KP50V2KX-1DLGP
SC1KP50V2KX-1DLGP

AUD_SPK_L-_C AUD_SPK_L+_C AUD_SPK_R-_C AUD_SPK_R+_C
AFTP2901
AFTP2902
AFTP2903
AFTP2904

20180911
Vendor modify

27 LINE1_VREFO
27 MIC2_VREFO_R
27,66 AUD_HP1_JACK_L
27,66 AUD_HP1_JACK_R
27 LINE1_L
27 LINE1_R
27,66 AUD_SLEEVE
27,66 AUD_RING
27,66 AUD_SENSE

LINE1_VREFO
D2901
BAW56-9-GP-U
75.00056.07D
LINE1_VREFO_L
LINE1_VREFO_R
RN2902
SRN4K7J-8-GP
RN2901
SRN2K2J-1-GP
MIC2_VREFO_R
AUD_RING
AUD_HP1_JACK_L
LINE1_L C29071 2 SC10U6D3V3MX-DL-GP
AUD_HP1_JACK_R
LINE1_R C29081 2 SC10U6D3V3MX-DL-GP
AUD_SLEEVE

20180911
Vendor modify

AUD_SENSE 10 mils
DY C2909
SC10U6D3V3MX-DL-GP
AUD_AGND

<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio IO

| Size | Document Number | Rev |
|---|---|---|
| A 4 | WASP 13" WHL-U | A00 |

Date: Thursday, March 07, 2019 Sheet 29 of 106

(Blanking)

<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

*(Reserved)*

| Size | Document Number | Rev |
|---|---|---|
| A 4 | WASP 13" WHL-U | A00 |

Date: Thursday, March 07, 2019 Sheet 30 o f 106

WWW.AliSaler.Com

# (Blanking)

<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

***LAN RTL8106***

| Size | Document Number | Rev |
|---|---|---|
| A 4 | ***WASP 13" WHL-U*** | ***A 00*** |

| Date: Thursday, March 07, 2019 | Sheet 31 o f 106 |
|---|---|

(Blanking)

<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

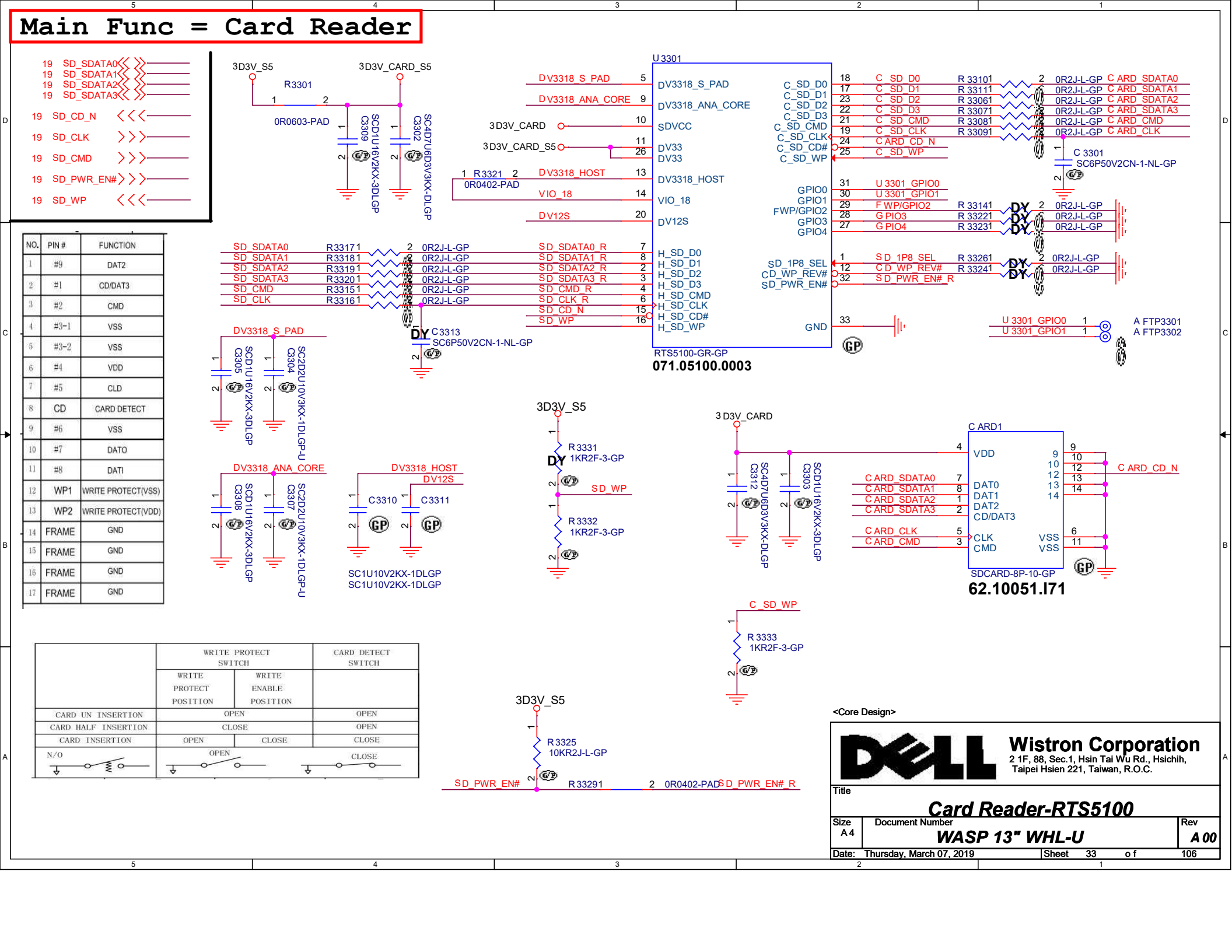
Title: XFOM&RJ45

| Size | Document Number | Rev |
|---|---|---|
| A 4 | WASP 13" WHL-U | A 00 |

Date: Thursday, March 07, 2019 | Sheet 32 of 106

WWW.AliSaler.Com

# Main Func = Card Reader




| NO. | PIN # | FUNCTION |
|---|---|---|
| 1 | #9 | DAT2 |
| 2 | #1 | CD/DAT3 |
| 3 | #2 | CMD |
| 4 | #3-1 | VSS |
| 5 | #3-2 | VSS |
| 6 | #4 | VDD |
| 7 | #5 | CLD |
| 8 | CD | CARD DETECT |
| 9 | #6 | VSS |
| 10 | #7 | DAT0 |
| 11 | #8 | DAT1 |
| 12 | WP1 | WRITE PROTECT(VSS) |
| 13 | WP2 | WRITE PROTECT(VDD) |
| 14 | FRAME | GND |
| 15 | FRAME | GND |
| 16 | FRAME | GND |
| 17 | FRAME | GND |

| | WRITE PROTECT SWITCH | | CARD DETECT SWITCH |
|---|---|---|---|
| | WRITE PROTECT POSITION | WRITE ENABLE POSITION | |
| CARD UN INSERTION | OPEN | | OPEN |
| CARD HALF INSERTION | CLOSE | | OPEN |
| CARD INSERTION | OPEN | CLOSE | CLOSE |
| N/O | OPEN | | CLOSE |

<Core Design>

**Wistron Corporation**
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Card Reader-RTS5100**

| Size | Document Number | Rev |
|---|---|---|
| A4 | WASP 13" WHL-U | A 00 |

Date: Thursday, March 07, 2019 | Sheet 33 of 106

# (Blanking)

<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)*

| Size | Document Number | Rev |
|---|---|---|
| A 4 | *WASP 13" WHL-U* | *A 00* |

Date: Thursday, March 07, 2019 | Sheet 34 of 106

WWW.AliSaler.Com

SSID = USB3.0

# (Blanking)

<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

**USB switch**

| Size | Document Number | Rev |
|---|---|---|
| | WASP 13" WHL-U | A 00 |

Date: Thursday, March 07, 2019 Sheet 3 5 o f 106

(Blanking)

<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
USB30

| Size | Document Number | Rev |
|---|---|---|
| A 4 | WASP 13" WHL-U | A 00 |

Date: Thursday, March 07, 2019 Sheet 36 o f 106

WWW.AliSaler.Com

# (Blanking)

<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

*(Reserved)*

| Size | Document Number | Rev |
|---|---|---|
| A 4 | *WASP 13" WHL-U* | *A 00* |

Date: Thursday, March 07, 2019 Sheet 37 o f 106

Main Func = USB3.0 Redriver

(Blanking)

<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

| | | |
|---|---|---|
| Title: USB30 | | |
| Size: A4 | Document Number: WASP 13" WHL-U | Rev: A 00 |
| Date: Thursday, March 07, 2019 | Sheet 38 of 106 | |

WWW.AliSaler.Com

# (Blanking)

<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

*(Reserved)*

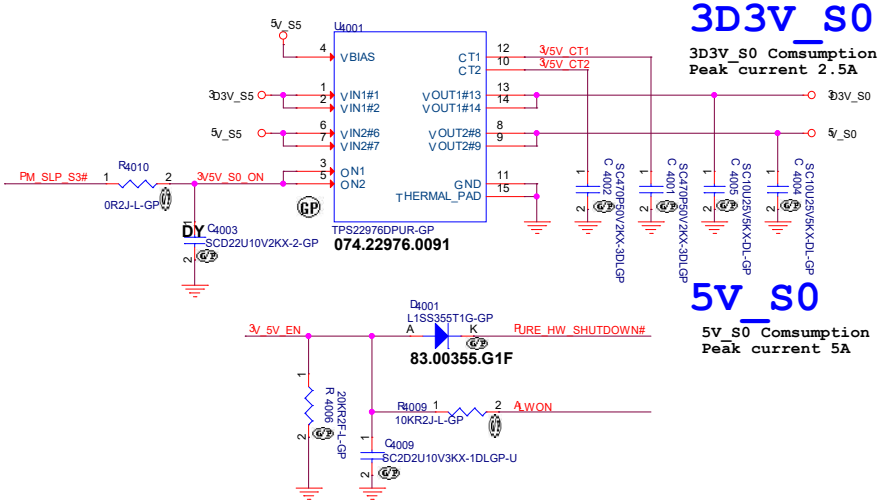
| Size | Document Number | Rev |
|---|---|---|
| A 4 | *WASP 13" WHL-U* | *A 00* |

Date: Thursday, March 07, 2019 Sheet 39 o f 106

# Main Func = Power Plane & Sequence

17 PM_SLP_S3#
17,24,46 VCCST_PWRGD
17,51,92 PM_SLP_S4#
17,91 PM_SLP_S0#
21 GPPC_H18_VCCIO_LPM
24 ALWON
24,53 PRIM_PWRGD
26 PURE_HW_SHUTDOWN#
45 3V_5V_EN
51 PWR_VDDQ_PG

## ROSA Run Power



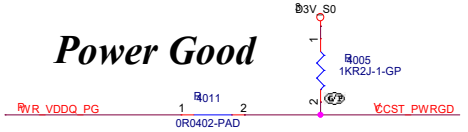

### 3D3V_S0

3D3V_S0 Comsumption
Peak current 2.5A

### 5V_S0

5V_S0 Comsumption
Peak current 5A

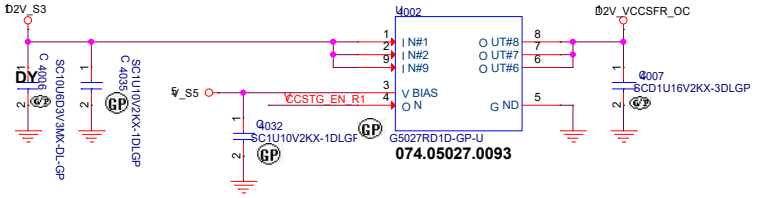
## Power Good




[#543016] Optional, Added for addition system robustness

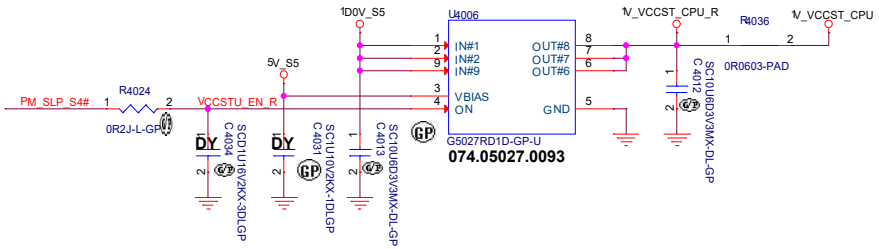
NON DS3: PH 3V_5V_POK to 3D3V_AUX_S5 at page17

## VCCSFR_OC

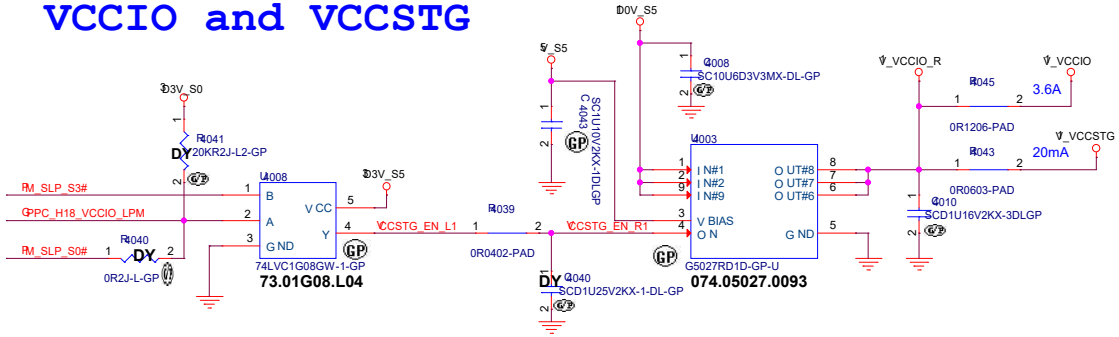



## MANAGEMENT RAIL POWER GENERATION

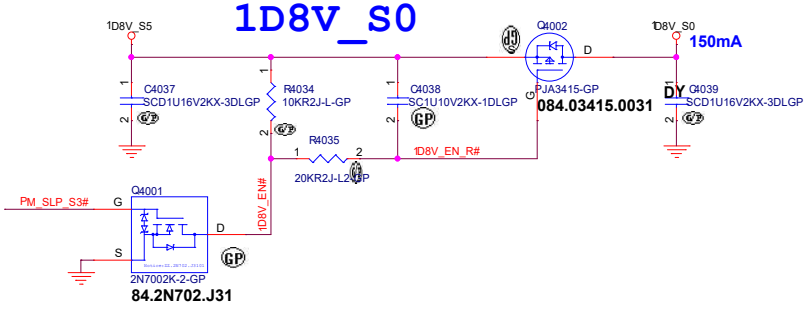
VCCST, VCCSTG, and VCCPLL can remain powered during S4 and S5 power states for board VR optimization.




## VCCIO and VCCSTG




## 1D8V_S0




<Core Design>

Wistron Corporation
2F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable

Size: A | Document Number: WASP 13" WHL-U | Rev: A00

Date: Thursday, March 07, 2019 | Sheet 40 of 106

WWW.AliSaler.Com

# (Blanking)

<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
*Connected_Standby(1/2)+DS3*

| Size | Document Number | Rev |
|---|---|---|
| A 4 | *WASP 13" WHL-U* | *A 00* |

Date: Thursday, March 07, 2019 Sheet 41 o f 106

(Blanking)

<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

| | | |
|---|---|---|
| Title | *Connected_Standby(2/2)* | |
| Size: A 4 | Document Number: WASP 13" WHL-U | Rev: A00 |
| Date: Thursday, March 07, 2019 | Sheet 42 of 106 | |

WWW.AliSaler.Com

# Main Func = ADT Input

24 PS_ID
24,44 AC_DIS
24,44 HW_ACAVIN_NB
24,44 PBAT_PRES#
24,44 PBAT_CHG_SMBCLK
24,44 PBAT_CHG_SMBDAT

PS_ID_R — C4309 SCD1U25V2KX-1DL-GP (DY) — 20180904 EMC add
+DC_IN_C — C4311 SC1KP50V2KX-1DLGP — JGND

**Layout Note:**
PSID Layout width > 25mil

R4302 15KR2F-GP — Q4302 LMBT3904LT1G-GP 84.T3904.H11
R4309 100KR2J-1-GP — Q4301 PJA138KA-GP 084.00138.0A31
R4303 10KR2J-L-GP — D4302 LBAV99LT1G-1-GP 75.00099.O7D
R4304 2K2R2J-2-GP — PS_ID
R4305 33R2J-2-GP — PS_ID_R1
R4306 33R2J-2-GP (DY)
R4317 0R0603-PAD — PS_ID_R2
D4303 L30ESD24VC3-2-GP 83.03024.0A1

DCIN1 ACES-CON8-GP-U2 20.F1295.008
EL4304 0R5J-5-GP — EL4303 0R5J-5-GP — AFTP4301 AFTP4302
60ohm@100MHz
DCR=0.02 ohm
Max current = 6000mA
EL4301 0R5J-5-GP — EL4302 0R5J-5-GP
D4301 P6AF24A-R1-00001-GP 083.00624.00AM
C4302 SCD1U25V2KX-1-DL-GP
C4301 SC1U25V2KX-1DLGP
R4307 240KR2-GP
R4308 47KR2F-GP

**S1**

Q4301 AONR21321-GP 084.21321.0037

Move S2 MOSFET and control logic SCH to page 44

9V_AD_JK — 9V_AD+
C4306 SC10U25V5KX-DL-GP
C4303 SCD1U25V2KX-3DLGP
C4304 SCD1U25V2KX-3DLGP
C4305 SCD1U25V2KX-3DLGP
R4316 20KR2J-L2-GP

Q4304 LMUN5212T1G-GP 84.05212.B11
Q4305 LMUN5112T1G-GP-U 084.05112.001K
AC_DIS — R4310 100KR2J-1-GP
AD_OFF_L — AD_OFF_R

AFTP4304 PS_ID_R
AFTP4303 AFTP4305 AFTP4316 +DC_IN_C

# Main Func = M-BAT Input

## Batt Connecter

PBAT_PRES1# KBC_SMB_SDA_BAT1 KBC_SMB_SCL_BAT1 BT+ BT+ BT+ — AFTP4309 AFTP4310 AFTP4311 AFTP4312 AFTP4313 AFTP4314
BT+ — C4308 SCD1U50V3KX-DL-GP (DY) — C4307 SC1KP50V2KX-1DLGP — D4304 SMF18A-GP
BATT1 ACES-CON12-12-GP-U1 20.F0818.012
PBAT_CHG_SMBCLK PBAT_CHG_SMBDAT — RN4302 SRN100J-3-GP
PBAT_PRES# — R4327 100R2J-2-GP
KBC_SMB_SCL_BAT KBC_SMB_SDA_BAT PBAT_PRES1#
C4309 SC10P50V2JN-4DLGP (DY) — C4310 SC10P50V2JN-4DLGP (DY) — C4306 SC10P50V2JN-4DLGP (DY)
AFTP4306 AFTP4307 AFTP4308

**Placement: Close to Batt Connector**

PBAT_PRES# — D4304 LBAV99LT1G-1-GP 75.00099.O7D (DY)
PBAT_CHG_SMBDAT — D4305 LBAV99LT1G-1-GP 75.00099.O7D (DY)
PBAT_CHG_SMBCLK — D4306 LBAV99LT1G-1-GP 75.00099.O7D (DY)
3V_S5_KBC

# Barrel Adapter Piug-in Detect

9V_AD_JK — R4376 47KR2F-GP — R4377 84K5R2F-GP
3V_S5 — R4378 100KR2J-1-GP — HW_ACAVIN_NB
AC_IN#_G — C_DELAY — C4344 SC1KP50V2KX-1DLGP
U4302 ST1004NA23I-M5T1U-GP 074.01004.00BF (S ENSE, C D, O UT, V DD, V SS)

<Core Design>

Wistron Corporation
2F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DCIN
Size: B | Document Number: WASP 13" WHL-U | Rev: A00
Date: Thursday, March 07, 2019 | Sheet 43 of 106

Main Func = Charger

# ISL9538H For Charger

OFFPAGE

From MCP_ACK

| | ISL9538H | ISL95522 |
|---|---|---|
| PR4468 | 100K(63.10434.10L) | 100K(64.R0005.6DL) |
| PC4469 | 1500p(78.15224.2FLDL) | DY |
| PQ4451 | 084.02421.0031 | DY |
| PR4469 | DY | 0R(64.R0005.6DL) |
| PR4441 | DY | 0R(64.R0005.6DL) |
| PR4440 | 0R(64.R0005.6DL) | DY |
| PR4471 | 0R(64.R0005.6DL) | DY |
| PR4470 | DY | 0R(64.R0005.6DL) |

S2

084.21321.0037

75.27002.F7C

75.00054.A7D

83.R2003.A8M

068.2R210.2351
10mm x 11.2mm
x 2mm
DCR=8~9mohm
Idm=13A
Iset=10A

075.07321.0073

084.03305.0037

## +3D3V_VDD_DCIN

20V>+DC_IN>4.7V

Vout=1.24*(1+(R1/R2))

74.02204.03F

## Vcore_OVP

Trigger Voltage
VDD=4.5V, Vcore > 1.88V
VDD= 5V, Vcire > 2.084V
VDD=5.5V, Vcire > 2.3V

74.00331.H2F

83.00355.G1F

## Vsys_UVP

Trigger Voltage
VDD=4.5V, DCBATOUT < 5.39V
VDD= 5V, DCBATOUT < 5.98V
VDD=5.5V, DCBATOUT < 6.58V

74.00331.H2F

83.00355.G1F

PU +VCCSTG = 1.0 V on CPU side

84.2N702.J31

Barrel Prochot
Follow custormer circuits.

TypeC Prochot
Follow custormer circuits.

84.2N702.J31

Wistron Corporation

Power (Charger_ISL9538)

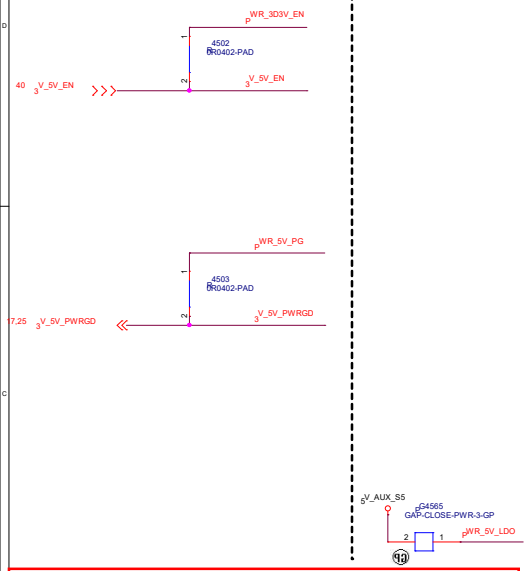
W ASP 13" WHL-U

WWW.AliSaler.Com

SSID = PWR.Plane.Regulator_5V

OFFPAGE-Signal

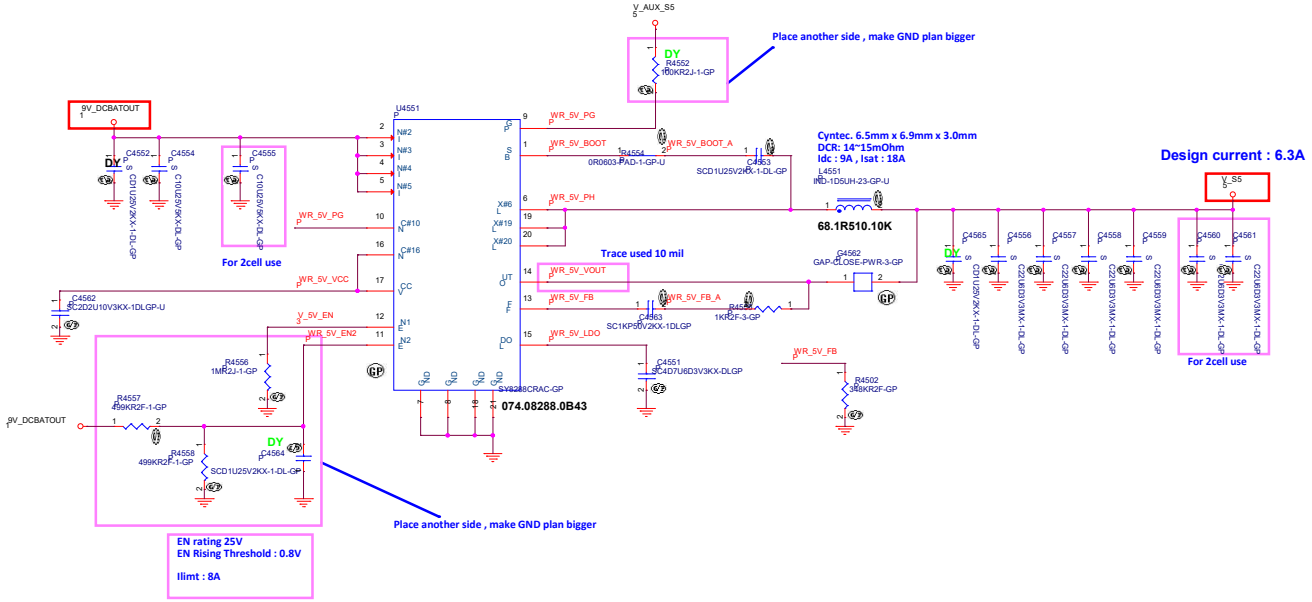
OFFPAGE-GAP







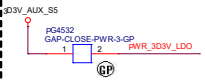
# SY8288C For 5V



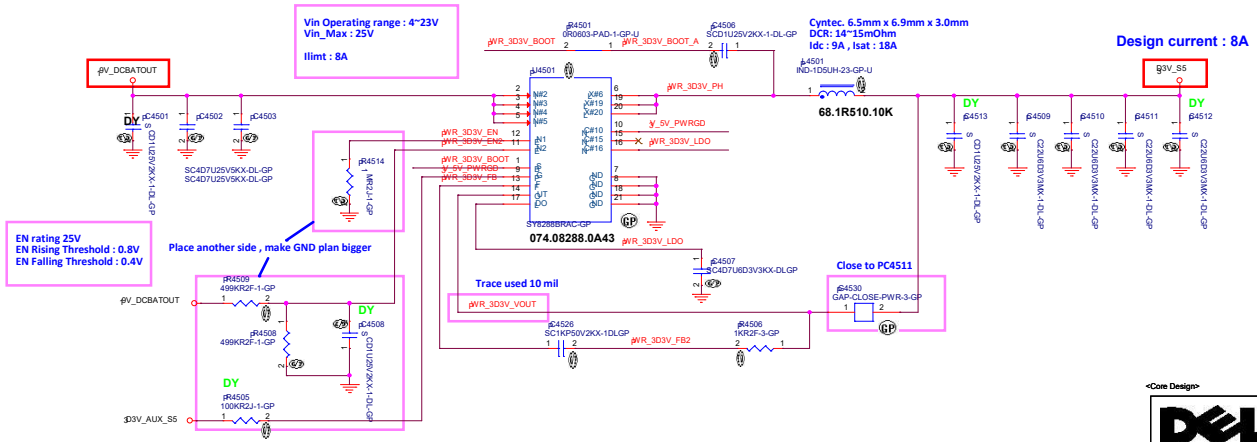

SSID = PWR.Plane.Regulator_3D3V

OFFPAGE-Signal

OFFPAGE-GAP




# SY8288B For 3D3V




<Core Design>

Wistron Corporation
3F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (SY8288_5V/3D3V)

Size: A | Document Number: WASP 13" WHL-U | Rev: A0

Date: Thursday, March 07, 2019 | Sheet 45 of 108

Main Func = CPU_CORE

OFFPAGE

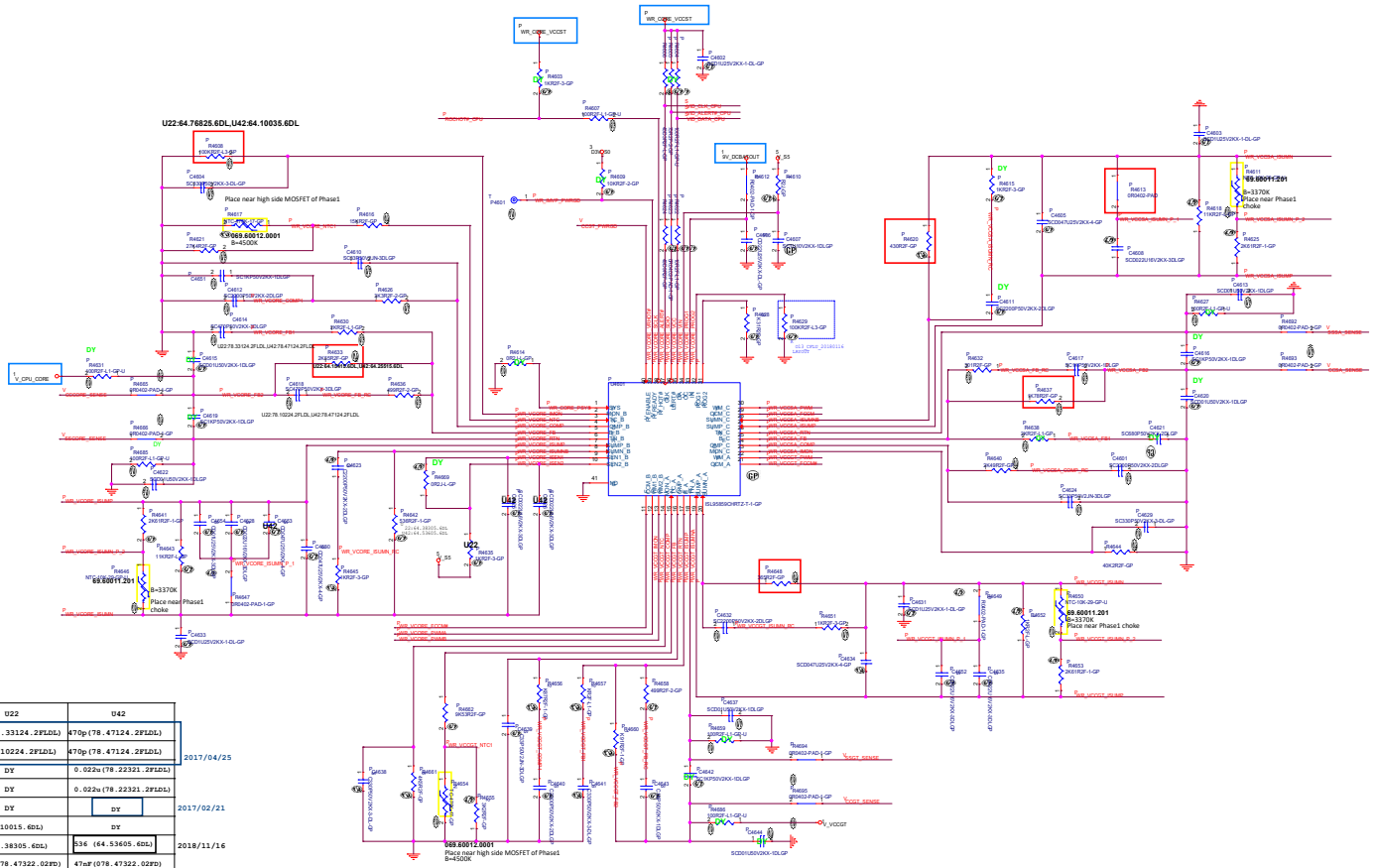
# ISL95859C For CPUCORE

PH on CPU side

For VCCGT Sense

For Vcore Sense

EE side Link
SVID Pull High V




| | U22 | U42 | |
|---|---|---|---|
| PC4614 | 330P(78.33124.2FLDL) | 470p(78.47124.2FLDL) | |
| PC4618 | 1KP(78.10224.2FLDL) | 470p(78.47124.2FLDL) | 2017/04/25 |
| PC4625 | DY | 0.022u(78.22321.2FLDL) | |
| PC4626 | DY | 0.022u(78.22321.2FLDL) | |
| PR4669 | DY | DY | 2017/02/21 |
| PR4635 | 1K(64.10015.6DL) | DY | |
| PR4642 | 383(64.38305.6DL) | 536 (64.53605.6DL) | 2018/11/16 |
| PC4630 | 47nF(078.47322.02FD) | 47nF(078.47322.02FD) | |
| PC4628 | 22nF(78.22321.2FLDL) | 22nF(78.22321.2FLDL) | |
| PC4654 | 10nF(78.10322.2FLDL) | 10nF(78.10322.2FLDL) | |
| PC4653 | DY | 47nF(078.47322.02FD) | |
| PR4633 | 1.54K(64.15415.6DL) | 2.55K(64.25515.6DL) | |
| PR4608 | 76.8K(64.76825.6DL) | 100K (64.10035.6DL) | |

Wistron Corporation
2F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

POWER (95859_CPUCORE(1/3))

Size: A | Document Number: W ASP 13" WHL-U | Rev: A0

Date: Thursday, March 07, 2019 | Sheet 45 of 106

WWW.AliSaler.Com

Main Func = CPU_CORE

# AOZ5038Q For VCORE

## OFFPAGE

9V_DCBATOUT — L4703 HCB2012KF-600T50-GP-U — L4704 HCB2012KF-600T50-GP-U — WR_DCBATOUT_VCOREA

46 WR_VCORE_PWMA
46 WR_VCORE_PWMB
46 WR_VCORE_FCCM#
46 WR_VCORE_ISEN1
46 WR_VCORE_ISEN2
46 WR_VCORE_ISUMP
46 WR_VCORE_ISUMN

For acoustic noise

WR_DCBATOUT_VCOREA — C4702 SE33U25VM-11-GP — 79.33612.20L

5V_S5 — C4777 SC2D2U6D3V2MX-DL-GP — R4703 2D2R2F-GP — WR_VCORE_VCCDA — C4709 SC2D2U6D3V2MX-DL-GP

U4701 AOZ5038QI-05-GP 074.05038.0A73

WR_VCORE_PWMA — R4702 0R0402-PAD-1-GP — WR_VCORE_PWMA_RA
WR_VCORE_FCCM# — R4706 0R0402-PAD-1-GP — WR_VCORE_FCCM#_RA
R4717 5K11R2F-L1-GP DY

WR_DCBATOUT_VCOREA — C4702 C4703 C4704 DY C4705 — WR_VCORE_BOOTA_RC — R4704 2D2R3F-L-GP — C4708 SCD22U25V3KX-DL-GP

SC10U25V3MX-5-GP ×4

WR_VCORE_BOOTA — WR_VCORE_BOOTRA — WR_VCORE_SWA

R4705 2D2R6J-3-GP DY — WR_VCORE_SNB1 — C4710 SC1KP50V2KX-1DLGP DY

WHL_U42_15W
Icc(max)=70A
TDC=48A

Cyntec 6.8mmx7.6mmx3.0mm
DCR: 0.9m ohm +/-7%
Idc : 38A , Isat : 45A

L4701 IND-D15UH-33-GP 068.R1510.1171

V_CPU_CORE — C4708 GAP-CLOSE-PWR-3-GP — C4709 GAP-CLOSE-PWR-3-GP — T4703 SE330U2VDM-4-GP 79.33719.20C

WR_VCORE_ISUMP_GA — WR_VCORE_ISUMN_GA

WR_VCORE_ISEN1 — R4721 100KR2F-L3-GP — U42
WR_VCORE_ISUMP — R4708 3K65R2F-1-GP — U42
WR_VCORE_ISUMN — R4709 10R2F-L1-GP — U42
WR_VCORE_ISEN2 — R4722 100KR2F-L3-GP DY — U42

5V_S5 — U42 C4766 SC2D2U6D3V2MX-DL-GP — R4713 2D2R2F-GP — WR_VCORE_VCCDB — U42 C4712 SC2D2U6D3V2MX-DL-GP

U4702 AOZ5038QI-05-GP 074.05038.0A73

WR_VCORE_PWMB — R4711 0R0402-PAD-1-GP — WR_VCORE_PWMB_RA
WR_VCORE_FCCM# — R4712 0R0402-PAD-1-GP — WR_VCORE_FCCM#_RB
R4718 5K11R2F-L1-GP DY

WR_DCBATOUT_VCOREA — U42 C4716 C4717 DY C4714 C4715 — WR_VCORE_BOOTB_RC — R4710 2D2R3F-L-GP — U42 C4711 SCD22U25V3KX-DL-GP

SC10U25V3MX-5-GP ×4

WR_VCORE_BOOTB — WR_VCORE_BOOTRB — WR_VCORE_SWB

R4714 2D2R6J-3-GP DY — WR_VCORE_SNB2 — C4713 SC1KP50V2KX-1DLGP DY

Cyntec 6.8mmx7.6mmx3.0mm
DCR: 0.9m ohm +/-7%
Idc : 38A , Isat : 45A

U42 L4702 IND-D15UH-33-GP 068.R1510.1171

V_CPU_CORE — C4713 GAP-CLOSE-PWR-3-GP — C4715 GAP-CLOSE-PWR-3-GP — U42 T4701 SE330U2VDM-4-GP 79.33719.20C

WR_VCORE_ISUMP_GB — WR_VCORE_ISUMN_GB

WR_VCORE_ISEN2 — R4723 100KR2F-L3-GP — U42
WR_VCORE_ISUMP — R4716 3K65R2F-1-GP — U42
WR_VCORE_ISUMN — R4715 10R2F-L1-GP — U42
WR_VCORE_ISEN1 — R4724 100KR2F-L3-GP DY — U42

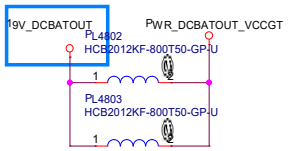
Wistron Corporation
2F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

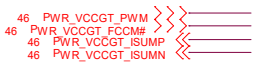
Title: POWER (5038_CPU_VCORE(2/3))
Size: Custom | Document Number: WASP 13" WHL-U | Rev: A00
Date: Thursday, March 07, 2019 | Sheet 47 of 106

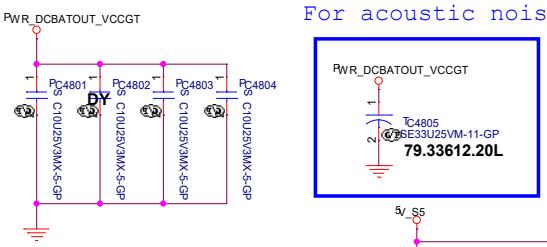
Main Func = CPU_CORE

# AOZ5038Q For VCCGT

Offpage-Signal

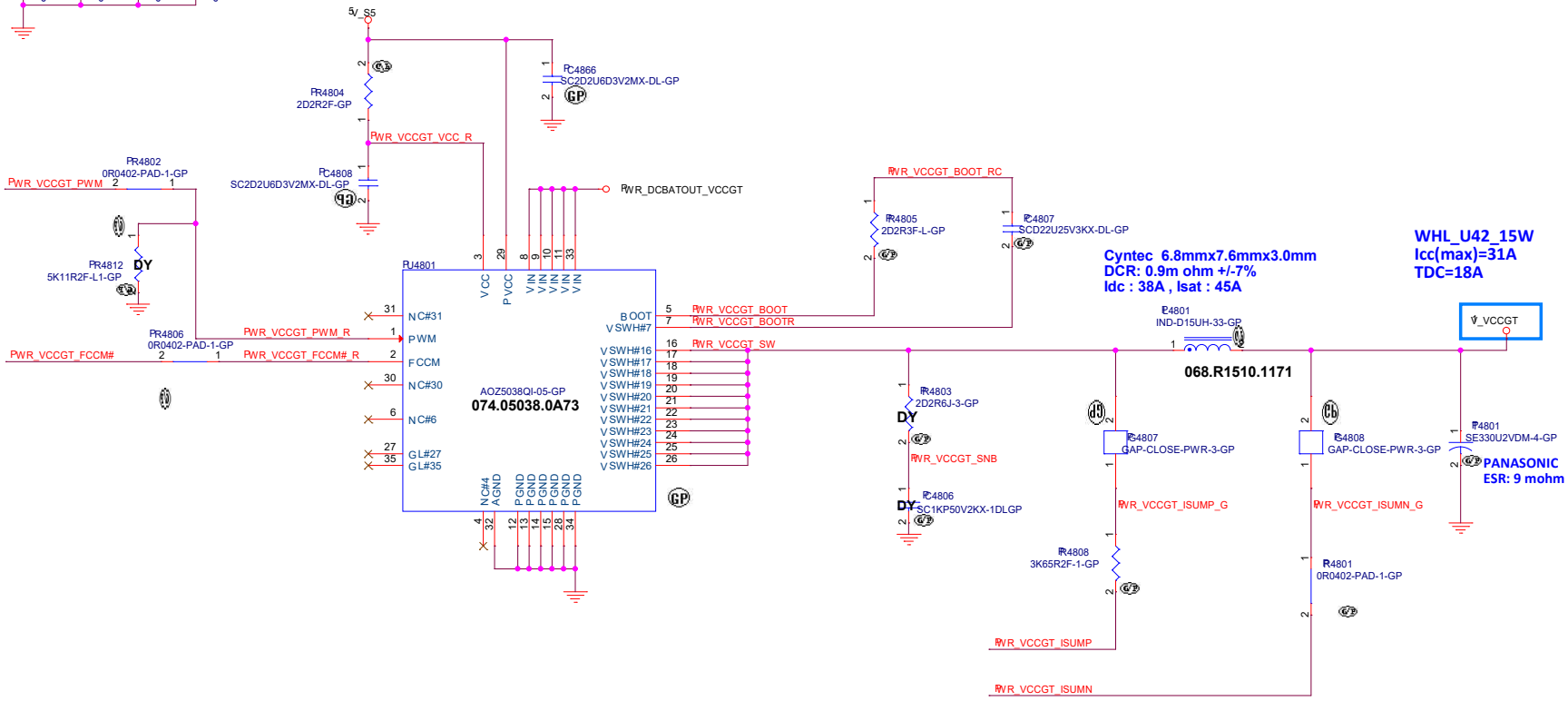



For acoustic noise




| | | | |
|---|---|---|---|
| Wistron Corporation<br>2F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. | | | |
| Title: POWER (5038_CPU_VCORE(3/3)) | | | |
| Size: B | Document Number: WASP 13" WHL-U | | Rev: A00 |
| Date: Thursday, March 07, 2019 | Sheet 48 of 106 | | |

WWW.AliSaler.Com

# RSVD

<Core Design>

Wistron Corporation
2F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (CPU_VCCGTS_RSVD)

Size: B | Document Number: WASP 13" WHL-U | Rev: A00

Date: Thursday, March 07, 2019 | Sheet 49 of 106

**Main Func = CPU_CORE**

# ISL95808 For VCCSA

## OFFPAGE

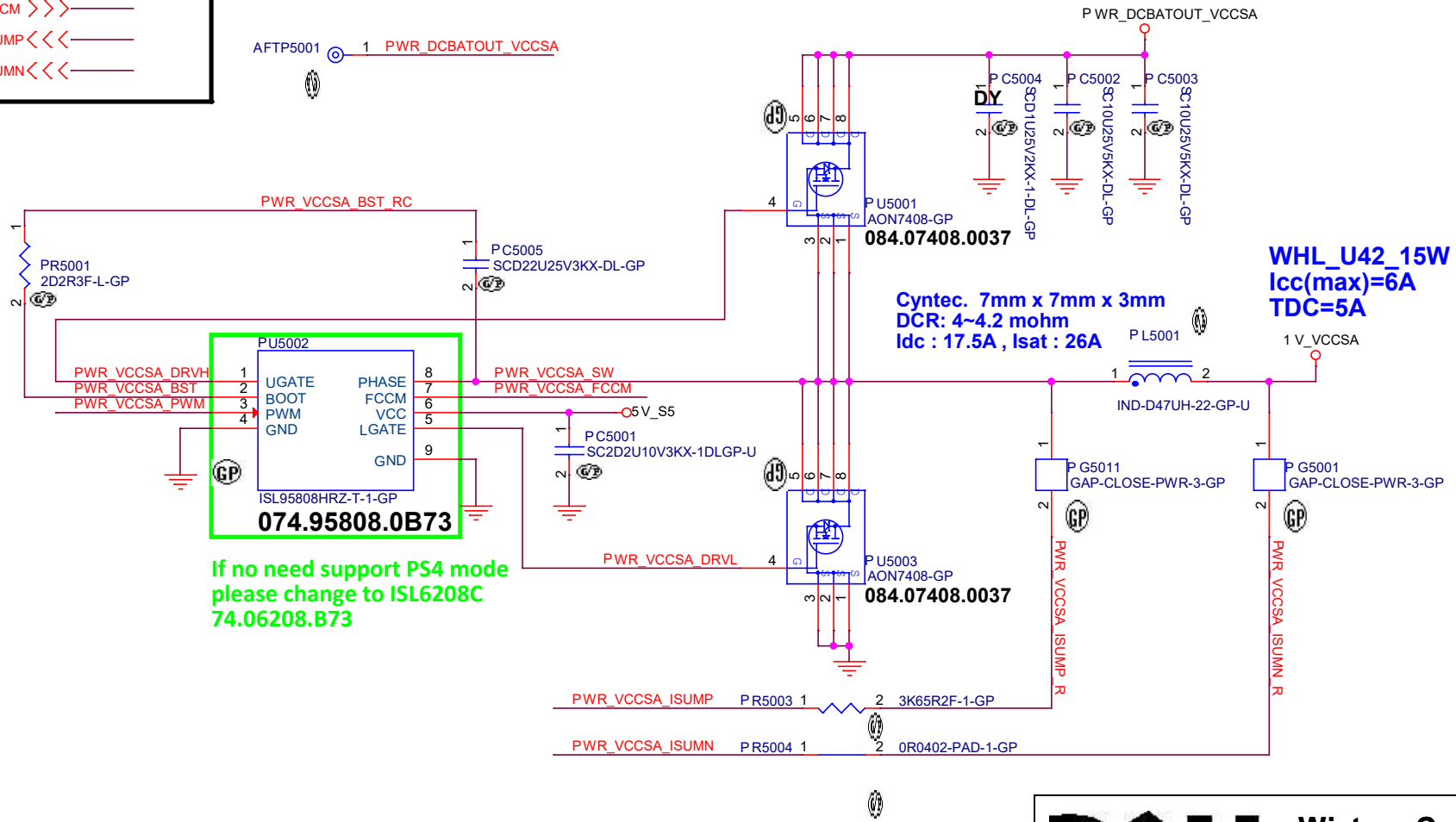
19V_DCBATOUT — R5001 (0R6J-L-GP) — PWR_DCBATOUT_VCCSA

46 PWR_VCCSA_PWM >>>

46 PWR_VCCSA_FCCM >>>

46 PWR_VCCSA_ISUMP <<<

46 PWR_VCCSA_ISUMN <<<





Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.


Title: **POWER (ISL95808_VCCSA)**

| Size | Document Number | Rev |
|---|---|---|
| A4 | WASP 13" WHL-U | A 00 |

Date: Thursday, March 07, 2019 Sheet 50 of 106

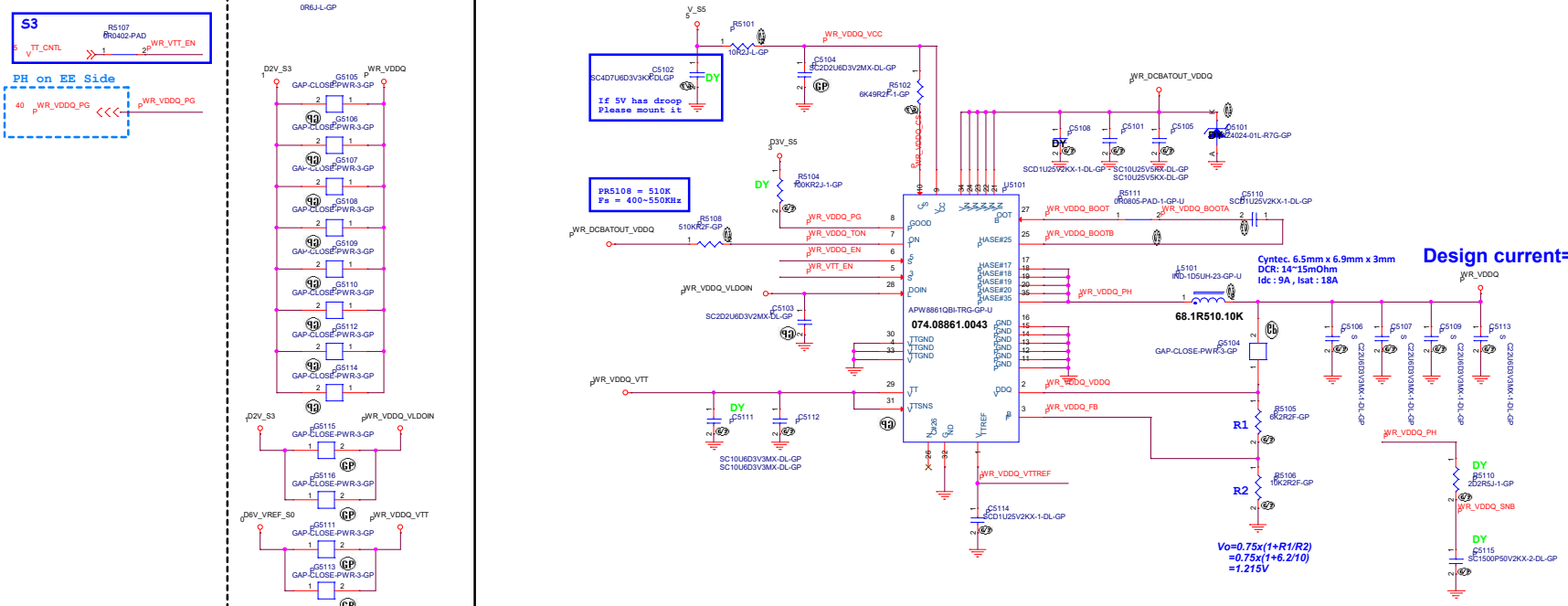
WWW.AliSaler.Com

SSID = PWR.Plane.Regulator_1D2V/0D6V

OFFPAGE-Signal

OFFPAGE-GAP

# G5388 For VDDQ/VTT



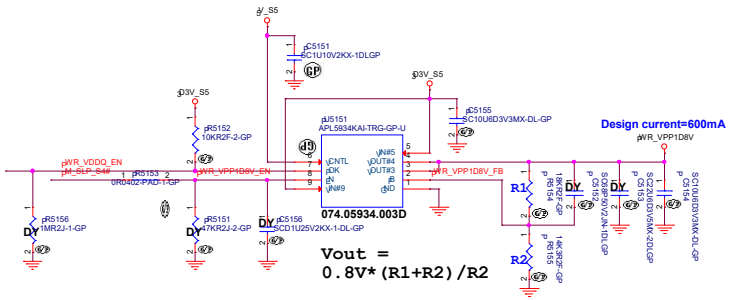

SSID = PWR.Plane.Regulator_1D8V

OFFPAGE-Signal

OFFPAGE-GAP

PH on EE Side

# APL5934 For 1D8V




<Core Design>

Wistron Corporation
3F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power (G5388_VDDQ_VTT_VPP)

Size: A | Document Number: WASP 13" WHL-U | Rev: A0

Date: Thursday, March 07, 2019 | Sheet 51 of 108

SSID = PWR.Plane.Regulator_1D0V

OFFPAGE-Signal

25,53 3V_5V_DSW_OK

# AOZ2262 For 1D0V

OFFPAGE-GAP

19V_DCBATOUT

PWR_DCBATOUT_1D05V

PG5201 GAP-CLOSE-PWR-3-GP

PG5202 GAP-CLOSE-PWR-3-GP

PG5203 GAP-CLOSE-PWR-3-GP

3D3V_S5

PR5208 100KR2J-1-GP

PWR_1D0V_PG

5V_S5

PC5202 SC4D7U25V5KX-DL-GP

PU5201

VCC

IN#7

IN#8

IN#9

TON

PGOOD

EN

PFM#

SS

LX#18

LX#17

LX#16

LX#11

LX#10

BST

FB

AGND

PGND

AOZ2262QI-10-2-GP

074.02262.M002

PWR_1D05V_PH

PWR_1D05V_BT

PWR_1D05V_VFB

PWR_1D05V_TON

PWR_1D0V_PG

PWR_1D05V_EN

PWR_1D05V_PFM

PWR_1D05V_SS

PR5201 95K3R2F-GP

PC5209

PC5210

SC10U25V5KX-DL-GP

SC10U25V5KX-DL-GP

3V_5V_DSW_OK PR5210 47KR2F-GP

PC5211 SCD1U16V2KX-3DLGP

PR5203 100KR2FL3-GP

PC5213 SCD01U25V2KX-3DLGP

Cyntec. 6.5mm x 6.9mm x 3mm
DCR: 9~10mOhm
Idc : 11A , Isat : 22A

PL5201 COIL-1UH-34-GP-U1

68.1R01A.20B

PC5204 SCD1U25V2KX-1-DL-GP

Design current =9.3A

1D0V_S5

PC5201 PC5203 PC5205 PC5207 PC5206

SC22U6D3V3MX-1-DL-GP
SC22U6D3V3MX-1-DL-GP
SC22U6D3V3MX-1-DL-GP
SC22U6D3V3MX-1-DL-GP
SC22U6D3V3MX-1-DL-GP

PG5210 GAP-CLOSE-PWR-3-GP

PWR_1D05V_VFB_A

PR5202 8K16R2F-GP

R1

PC5212 SC220P50V2KX-3DLGP

PR5204 10KR2F-2-GP

R2

Vo=0.8x(1+R1/R2)
=0.8x(1+3.16/10)
=1.0528V

<Core Design>

Wistron Corporation
2F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (AOZ2261Q_1D0V)

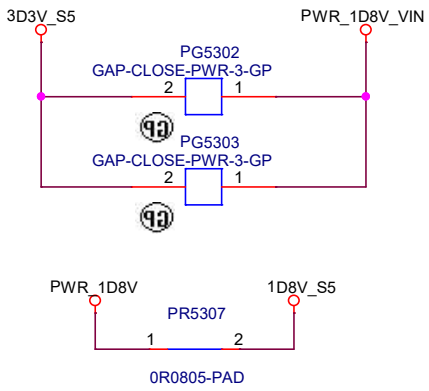
Size: B | Document Number: WASP 13" WHL-U | Rev: A00

Date: Thursday, March 07, 2019 | Sheet 52 of 106

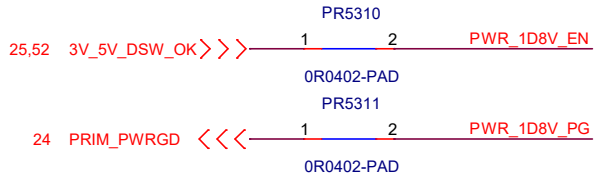
WWW.AliSaler.Com

# Main Func = 1D8V

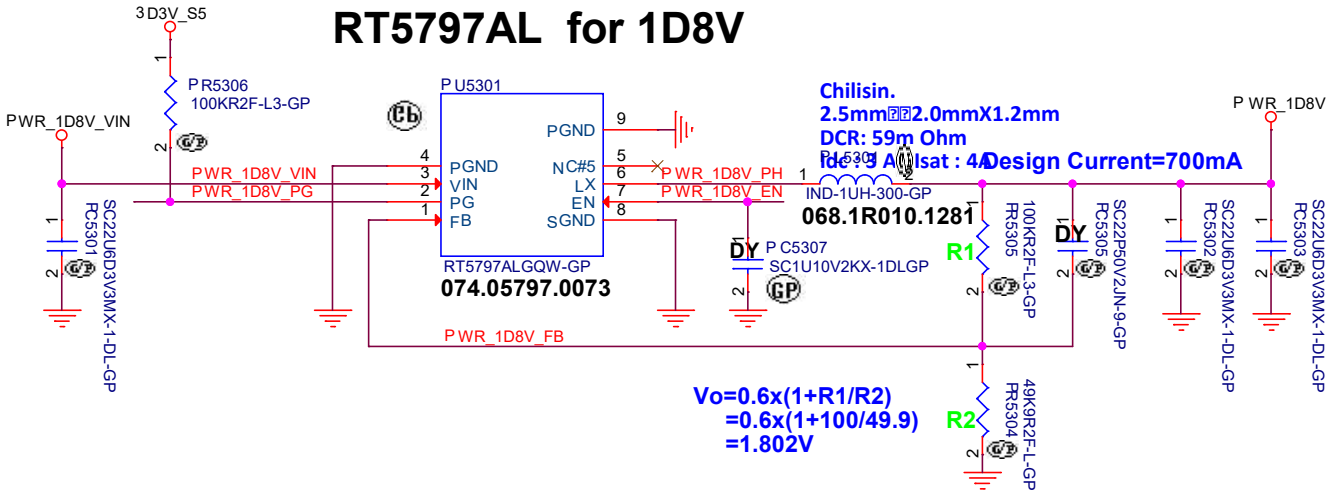
## OFFPAGE_GAP




## OFFPAGE




## RT5797AL for 1D8V




<Core Design>

**Wistron Corporation**
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

| | | |
|---|---|---|
| Title | POWER (APL5934_1D8V) | |
| Size: A4 | Document Number: WASP 13" WHL-U | Rev: A 00 |
| Date: Thursday, March 07, 2019 | Sheet 53 of 106 | |

# (Blanking)

<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

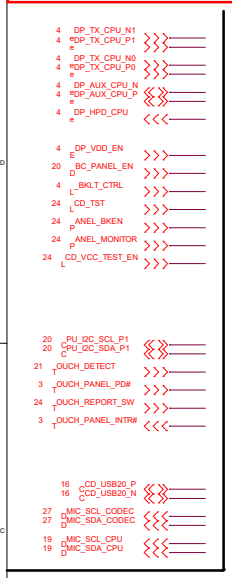
*(Reserved)*

| Size | Document Number | Rev |
|---|---|---|
| A 4 | *WASP 13" WHL-U* | *A 00* |

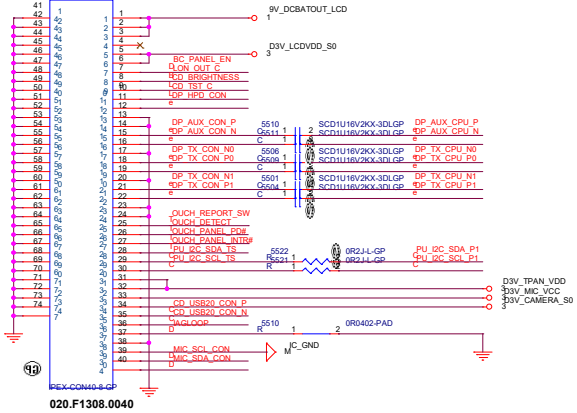
Date: Thursday, March 07, 2019 Sheet 54 o f 106

WWW.AliSaler.Com

# Main Func = LCD

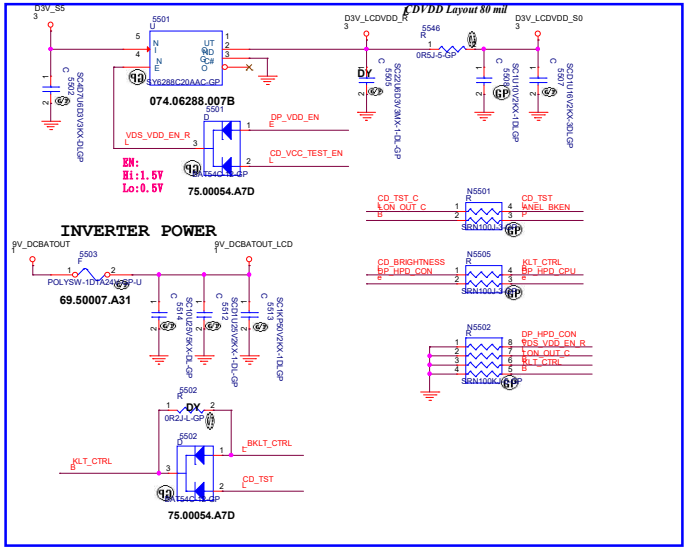



## eDP Panel / HD Camera



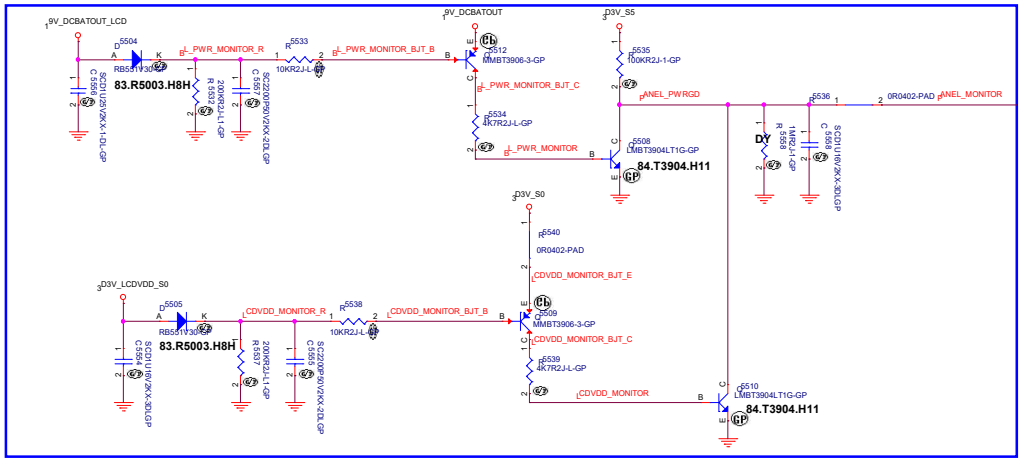

020.F1308.0040

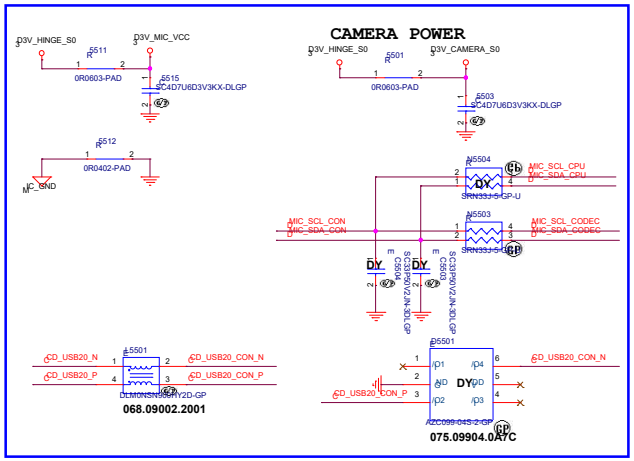
## D3V DD Layout 80 mil



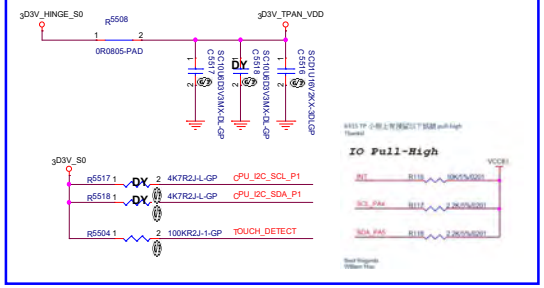

## M-BIST/ LCD BIST -20180425

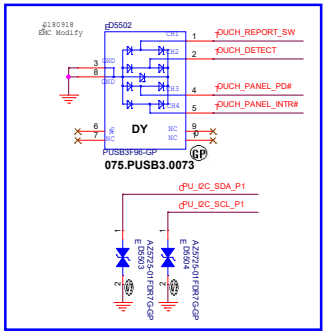
## LCD BIST for G10 (Was test only for G9)




## TOUCH PANEL POWER



<Core Design>
Wistron Corporation
3F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.


Title: LCD&CAM&DMC&Touch

Size: A | Document Number: WASP 13" WHL-U | Rev: A0

Date: Thursday, March 07, 2019 | Sheet 55 of 108

# (Blanking)

<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

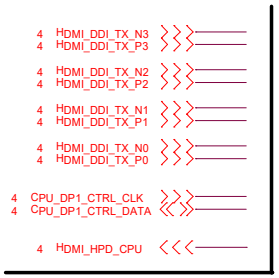
Title: CRT

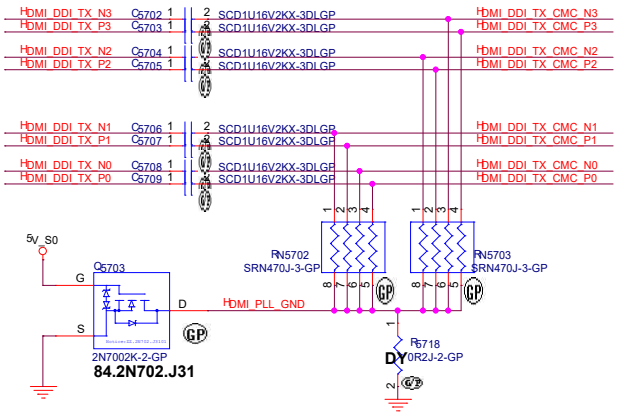
| Size | Document Number | Rev |
|---|---|---|
| A 4 | WASP 13" WHL-U | A 00 |

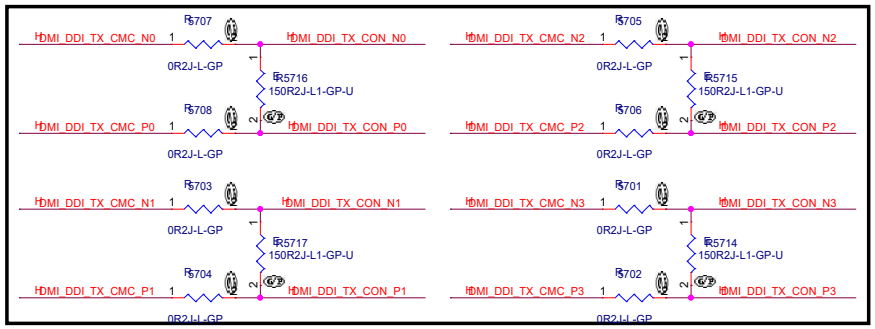
Date: Thursday, March 07, 2019 | Sheet 56 of 106

WWW.AliSaler.Com

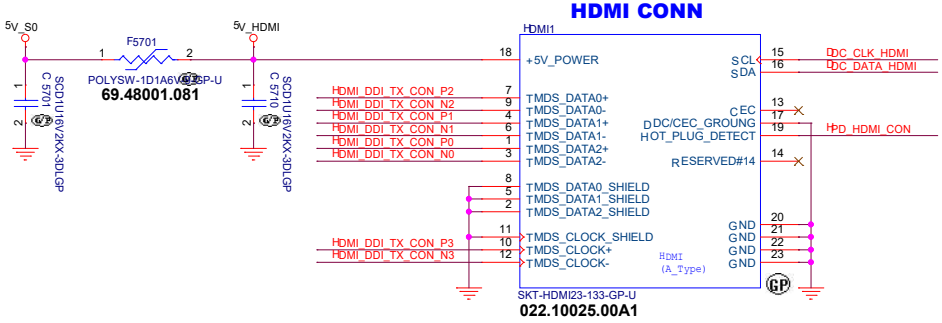
# Main Func = HDMI

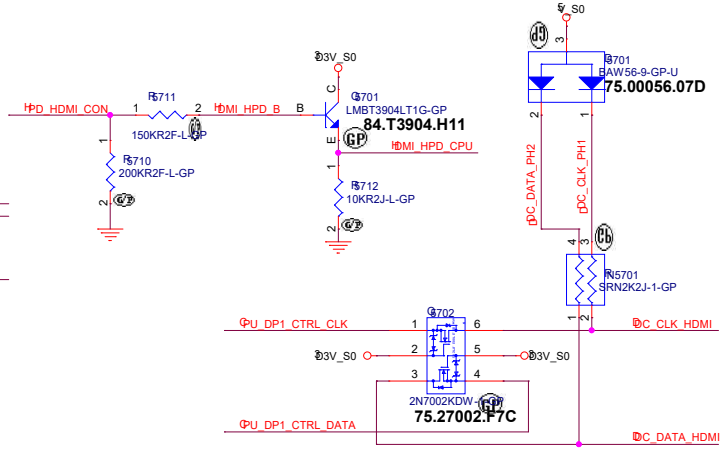


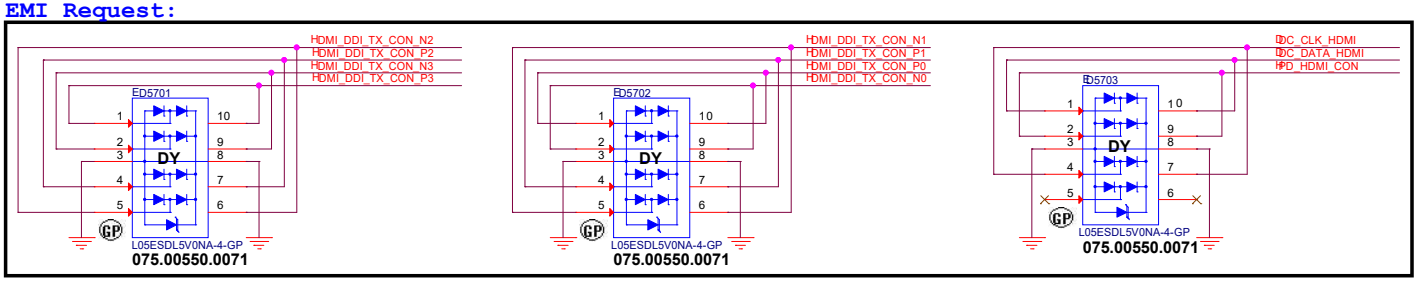




## HDMI CONN




## EMI Request:




<Core Design>

Wistron Corporation
2F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

| | | |
|---|---|---|
| Title | HDMI | |
| Size: B | Document Number: WASP 13" WHL-U | Rev: A00 |
| Date: Thursday, March 07, 2019 | Sheet 57 of 106 | |

# (Blanking)

<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
*(Reserved)*

| Size | Document Number | Rev |
|---|---|---|
| A 4 | *WASP 13" WHL-U* | *A 00* |

Date: Thursday, March 07, 2019 Sheet 58 o f 106

WWW.AliSaler.Com

# (Blanking)

<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
*(Reserved)*

| Size | Document Number | Rev |
|---|---|---|
| A4 | *WASP 13" WHL-U* | |

Date: Thursday, March 07, 2019 | Sheet 59 of 106

(Blanking)

<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SATA IF_HDD/ODD

| Size | Document Number | Rev |
|---|---|---|
| A 4 | WASP 13" WHL-U | A00 |

Date: Thursday, March 07, 2019 Sheet 60 o f 106

WWW.AliSaler.Com

# Main Func = WLAN

16 BT_USB20_N
16 BT_USB20_P
16 WLAN_PCIE_RX_N
16 WLAN_PCIE_RX_P
16 WLAN_PCIE_TX_N
16 WLAN_PCIE_TX_P
18 WLAN_CLK_CPU_N
18 WLAN_CLK_CPU_P
18 WLAN_CLKREQ_CPU_N
18 CLKIN_XTAL_LCP_R
20 CNV_BRI_DT
20 CNV_RGI_RSP
15,20 CNV_RGI_DT
20 CNV_BRI_RSP
21 CNV_WT_CLK_DP
21 CNV_WT_CLK_DN
21 CNV_WT_DP0
21 CNV_WT_DN0
21 CNV_WT_DP1
21 CNV_WT_DN1
21 CNV_WR_CLK_DP
21 CNV_WR_CLK_DN
21 CNV_WR_DP0
21 CNV_WR_DN0
21 CNV_WR_DP1
21 CNV_WR_DN1
66 CNV_MFUART2_TXD
66 CNV_MFUART2_RXD
66 CNV_COEX3
17,63,66,76,91 PLTRST#_CPU
18,24 SUS_CLK
18 JIO3_PCIE_WAKE#
19 BT_PCMFRM_RSTN
19 BT_PCMOUT_CLKREQ0
21 BLUETOOTH_EN
21 WIFI_RF_EN

3D3V_S5 — R6114 — 3D3V_WLAN
1 — 2
0R0805-PAD

W LAN1

3D3V_WLAN
76 76
74
72 3_3VAUX
70 3_3VAUX
68 RESERVED#70
66 RESERVED#68
64 RESERVED#66
CLKIN_XTAL_LCP 62 GPIO0_NFC_RESET#/MGPIO7
60 NFC_I2C_IRQ/MGPIO5
58 NFC_I2C_SM_CLK
56 NFC_I2C_SM_DATA
WIFI_RF_EN_R 54 W_DISABLE#1
BLUETOOTH_EN_R 52 RESERVED#54/W_DISABLE#2
PLTRST#_CPU 50 PERST0#
SUSCLK_WLAN 48 SUSCLK_32KHZ
WLAN_COEX1 46 COEX1
WLAN_COEX2 44 COEX2
WLAN_COEX3 42 COEX3
40 CLINK_CLK
38 CLINK_DATA
CNV_BRI_DT_R 36 CLINK_RESET
CNV_RGI_RSP_R 34 UART_CTS
CNV_RGI_DT_R 32 UART_RTS
UART_TX
CNV_BRI_RSP_R 22
20 UART_RX
18 UART_WAKE
16 GND
BT_PCMOUT_CLKREQ0 14 LED#2
12 PCM_OUT
BT_PCMFRM_RSTN 10 PCM_IN
8 PCM_SYNC
6 PCM_CLK
4 LED#1
3D3V_WLAN 2 3_3VAUX
NP2 NP2

77 77
75 GND
73 RESERVED#73
71 RESERVED#71
69 GND
67 RESERVED#67/2ND_LANE_PERN1
65 RESERVED#65/2ND_LANE_PERP1
63 GND
61 RESERVED#61/2ND_LANE_PETN1
59 RESERVED#59/2ND_LANE_PETP1
57 GND
55 PEWAKE0#
53 CLKREQ0#
51 GND
49 REFCLKN0
47 REFCLKP0
45 GND
43 PERN0
41 PERP0
39 GND
37 PETN0
35 PETP0
33 GND
23 SDIO_RESET
21 SDIO_WAKE
19 SDIO_DAT3
17 SDIO_DAT2
15 SDIO_DAT1
13 SDIO_DAT0
11 SDIO_CMD
9 SDIO_CLK
7 GND
5 USB_D-
3 USB_D+
1 GND
NP1 NP1

NGFF_KEY_E_75P
SKT-NGFF75P-70-GP-U1
062.10003.0401

C NV_WT_CLK_DP
C NV_WT_CLK_DN
C NV_WT_DP0
C NV_WT_DN0
C NV_WT_DP1
C NV_WT_DN1
J IO3_PCIE_WAKE#
W LAN_CLKREQ_CPU_N
W LAN_CLK_CPU_N
W LAN_CLK_CPU_P
W LAN_PCIE_RX_N
W LAN_PCIE_RX_P
W LAN_PCIE_TX_CON_N
W LAN_PCIE_TX_CON_P
C NV_WR_CLK_DP
C NV_WR_CLK_DN
C NV_WR_DP0
C NV_WR_DN0
C NV_WR_DP1
C NV_WR_DN1
B T_USB20_CON_N
B T_USB20_CON_P

SUS_CLK — R61171 — 2 — 33R2J-2-GP
CNV_MFUART2_RXD — R61071 — DY — 0R2J-L-GP — WLAN_COEX1
CNV_MFUART2_TXD — R61081 — DY — 0R2J-L-GP — WLAN_COEX2
CNV_COEX3 — R61091 — DY — 0R2J-L-GP — WLAN_COEX3

CNV_BRI_DT — R61111 — 2 — 33R2J-2-GP — CNV_BRI_DT_R
CNV_RGI_RSP — R61011 — 22R2J-L1-GP — CNV_RGI_RSP_R
CNV_RGI_DT — R61121 — 33R2J-2-GP — CNV_RGI_DT_R

CNV_BRI_RSP — R61021 — 2 — 22R2J-L1-GP — CNV_BRI_RSP_R

**Layout Note:**
R6101, R6102 Close to M.2 conn
R6111, R6112 Close to PCH

1D8V_S5
R61231 DY 2 20KR2J-L2-GP CNV_BRI_DT
R61221 DY 2 20KR2J-L2-GP CNV_RGI_RSP
R61211 DY 2 20KR2J-L2-GP CNV_BRI_RSP

**Layout Note:**
Close to M.2 conn
3D3V_WLAN
R61131 DY 2 10KR2J-L-GP WIFI_RF_EN_R
R61151 DY 2 10KR2J-L-GP BLUETOOTH_EN_R

R61191 2 71K5R2F-1-GP BT_PCMOUT_CLKREQ0
R61201 75KR2F-GP BT_PCMFRM_RSTN
R61181 2 10KR2J-L-GP CLKIN_XTAL_LCP
R61031 2 100KR2J-1-GP PLTRST#_CPU

**Layout Note:**
3D3V_WLAN
Close to M.2 conn pin2, pin4
C6104 SC10U6D3V3MX-DL-GP
C6105 SCD1U16V2KX-3DLGP
C6106 SCD01U25V2KX-3DLGP
3D3V_WLAN
Close to M.2 conn pin70, pin72
C6109 SC10U6D3V3MX-DL-GP
C6110 SCD1U16V2KX-3DLGP
C6111 SCD01U25V2KX-3DLGP

W IFI_RF_EN — R 61061 — DY — 2 — 0R2J-L-GP — W IFI_RF_EN_R
B LUETOOTH_EN — R 61101 — DY — 2 — 0R2J-L-GP — B LUETOOTH_EN_R
B T_USB20_CON_P — R 61051 — 2 — 0R0402-PAD — B T_USB20_P
B T_USB20_CON_N — R 61041 — 2 — 0R0402-PAD — B T_USB20_N
W LAN_PCIE_TX_CON_N — C 61071 — 2 — SCD1U16V2KX-3DLGP — W LAN_PCIE_TX_N
W LAN_PCIE_TX_CON_P — C 61081 — 2 — SCD1U16V2KX-3DLGP — W LAN_PCIE_TX_P
C LKIN_XTAL_LCP_R — R 61241 — 2 — 0R1J-GP — C LKIN_XTAL_LCP

AFTP6113 1 3D3V_WLAN
AFTP6108 1 PLTRST#_CPU
AFTP6112 1 BLUETOOTH_EN
AFTP6110 1 WIFI_RF_EN
AFTP6109 1 WLAN_CLKREQ_CPU_N
AFTP6111 1 BT_USB20_CON_N
AFTP6114 1 BT_USB20_CON_P
AFTP6115 1 JIO3_PCIE_WAKE#

<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NGFF_WLAN CONN
Size: A4 | Document Number: WASP 13" WHL-U | Rev: A 00
Date: Thursday, March 07, 2019 | Sheet 61 of 106

# (Blanking)

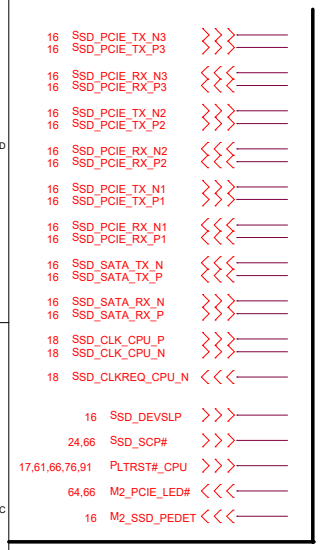
<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

| | | |
|---|---|---|
| Title: INT IO WWAN | | |
| Size: A4 | Document Number: WASP 13" WHL-U | Rev: A00 |
| Date: Thursday, March 07, 2019 | Sheet 62 of 106 | |

WWW.AliSaler.Com

# Main Func = SSD M.2



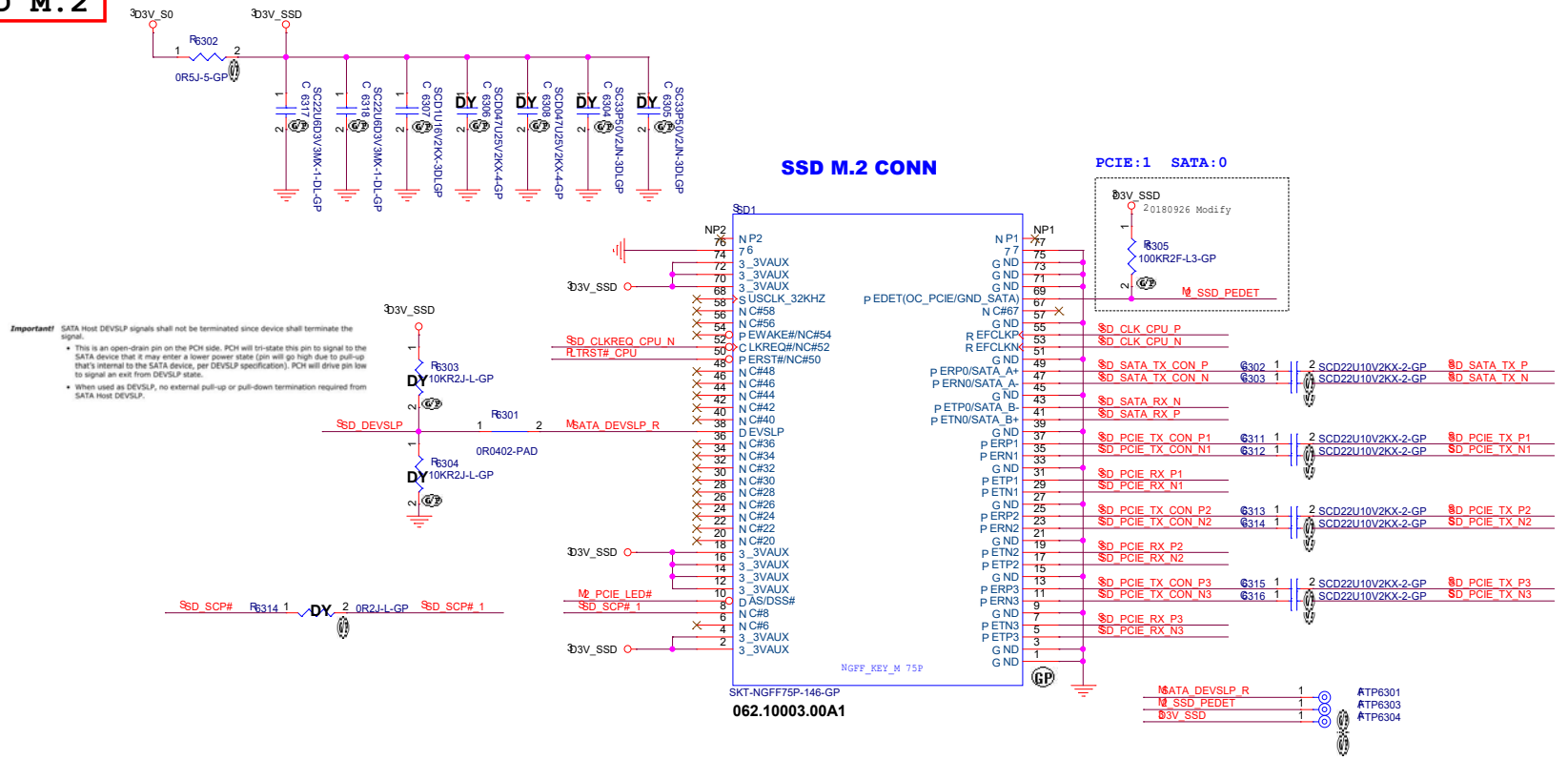




Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

## Table 13-11. SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

| Condition | PCI Express* Gen 2 Only | PCI Express* Gen 3 Only | SATA Only | PCI Express* Gen 2/ SATA | PCI Express* Gen 3/ SATA |
|---|---|---|---|---|---|
| Processor Tx | 100 nF | 220 nF | 10 nF | 100 nF | 220 nF |
| Processor Rx | None | None | 10 nF[2] | None | None[3] |

***Notes:***

1. Design Constraint: For PCIe only application, refer to the PCIe guidelines for details.
2. Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the Rx 10 nF capacitor can be removed if DC coupled ODDs / devices are NOT used.
3. Design Constraint: For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
4. Design Constraint: For PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
5. Design Constraints, Required: Refer to the Chapter 3, "General Differential Signals Design Guidelines"" along with the additional guidelines in this section for all design optimization guidelines.
6. Design Constraint: For PCIe* lane that needs to support either **PCIe* Gen2 devices** or **PCIe* Gen3 devices**, follow the PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**

<Core Design>

Wistron Corporation
2F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SSD M.2/eMMC

Size: B | Document Number: WASP 13" WHL-U | Rev: A00

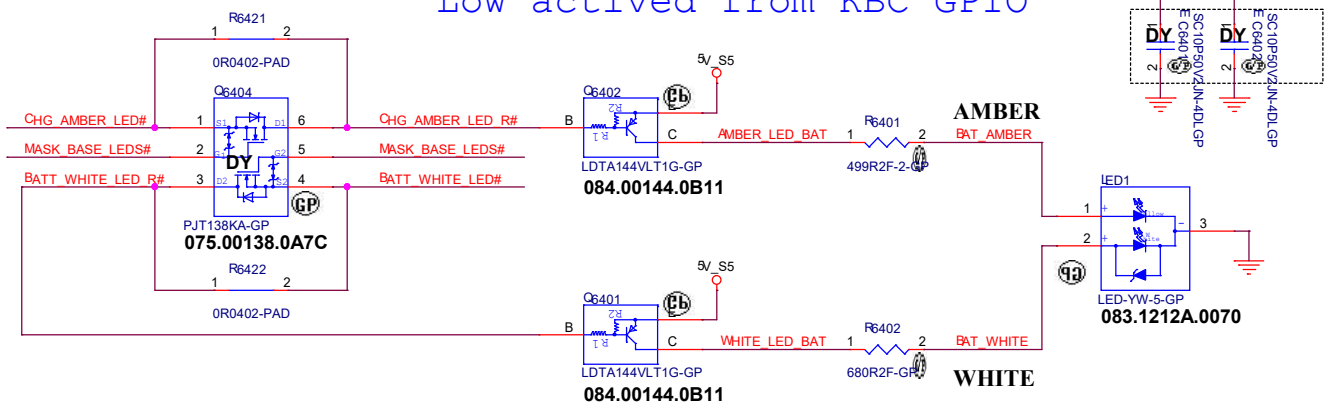
Date: Thursday, March 07, 2019 | Sheet 63 of 106

**Main Func = Power BTN**

| | |
|---|---|
| 24 | CHG_AMBER_LED# |
| 24 | BATT_WHITE_LED# |
| 24 | SYS_LED_MASK#_R |
| 16 | PCH_SATA_LED# |
| 63,66 | M2_PCIE_LED# |
| 20,24,67,92 | LID_CL_SIO# |
| 24 | MASK_SATA_LED# |
| 24,92 | KBC_PWRBTN# |
| 24,44 | HW_ACAV_IN |
| 17,24 | PCH_RSMRST# |
| 24 | EC_D_INHIB |

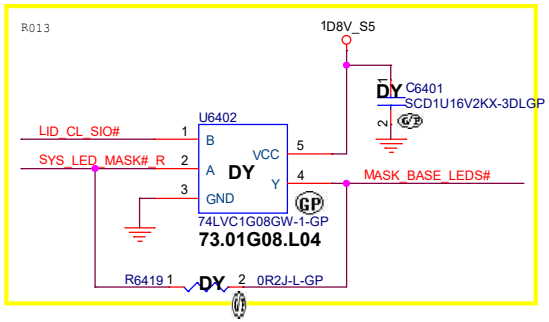
## Battery LED1 (AMBER_LED)

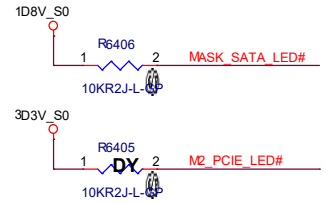
Low actived from KBC GPIO



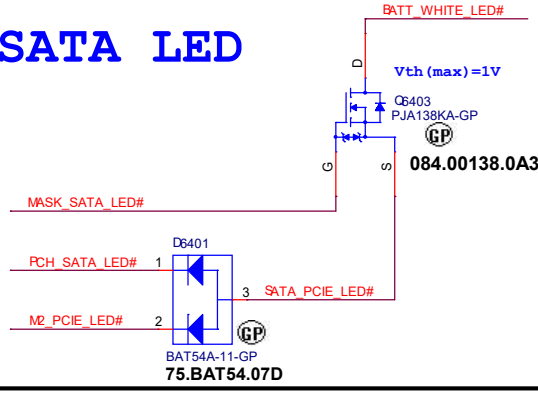

## Battery LED2 (WHITE_LED)

Low actived from KBC GPIO

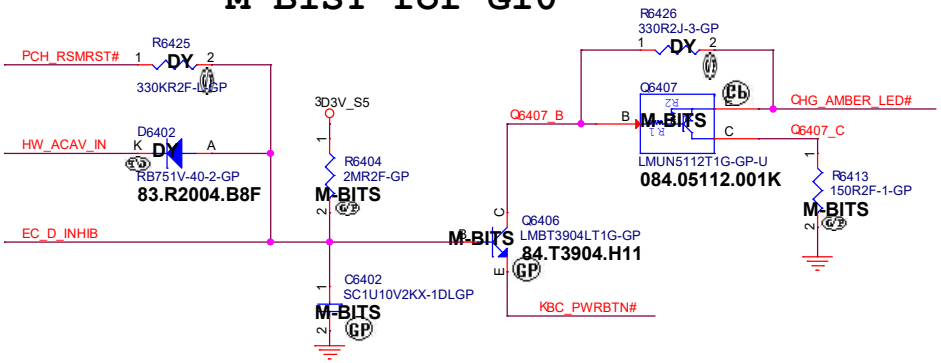



## SATA LED




## M-BIST for G10




M-BIST(Mainboard Built-In Self Test)Check if MB is damage while press power button. There is a LED will light up to indicate the MB is damage by

<Core Design>

Wistron Corporation
2F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

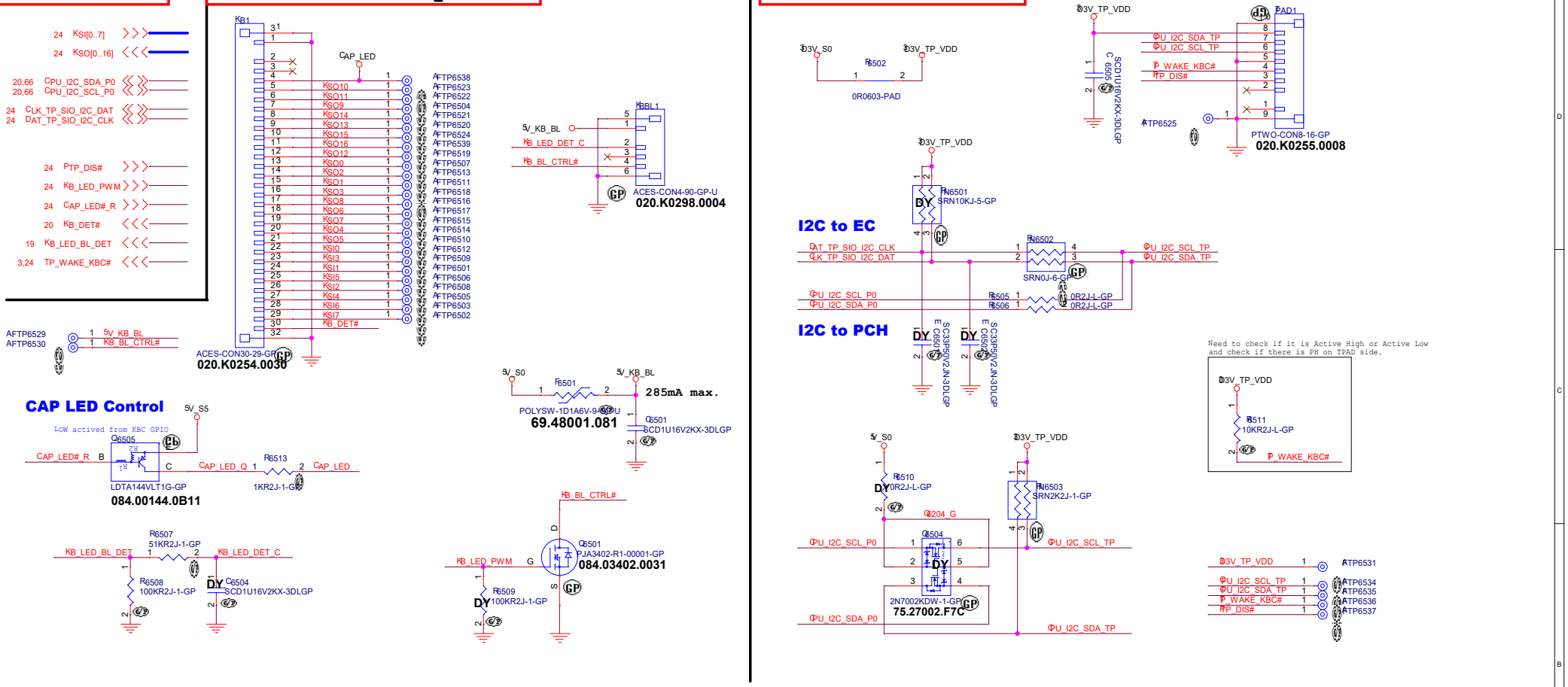
| | | |
|---|---|---|
| Title | LED Board&Power Button | |
| Size: Custom | Document Number: WASP 13" WHL-U | Rev: A00 |
| Date: Thursday, March 07, 2019 | Sheet 64 of 106 | |

WWW.AliSaler.Com

# SSID = KB

# Main Func = Keyboard

# Main Func = TPAD



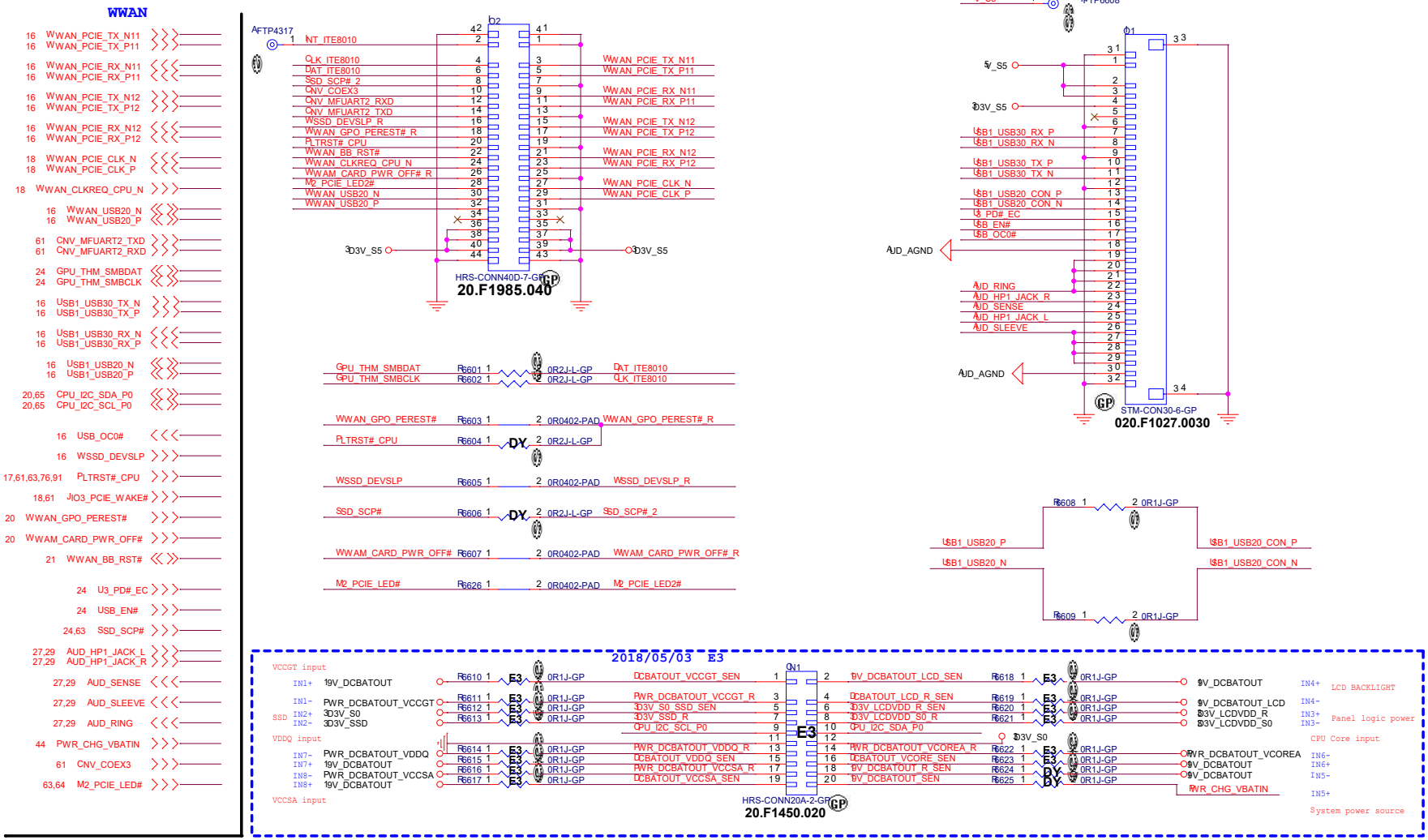

Wistron Corporation
2F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.


Title: **Key Board&Touch Pad**

Size: A | Document Number: **WASP 13" WHL-U** | Rev: **A00**

Date: Thursday, March 07, 2019 | Sheet 65 of 106

# Main Func = IO Connector




<Core Design>

Wistron Corporation
2F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board Connector

Size: A3 | Document Number: WASP 13" WHL-U | Rev: A00

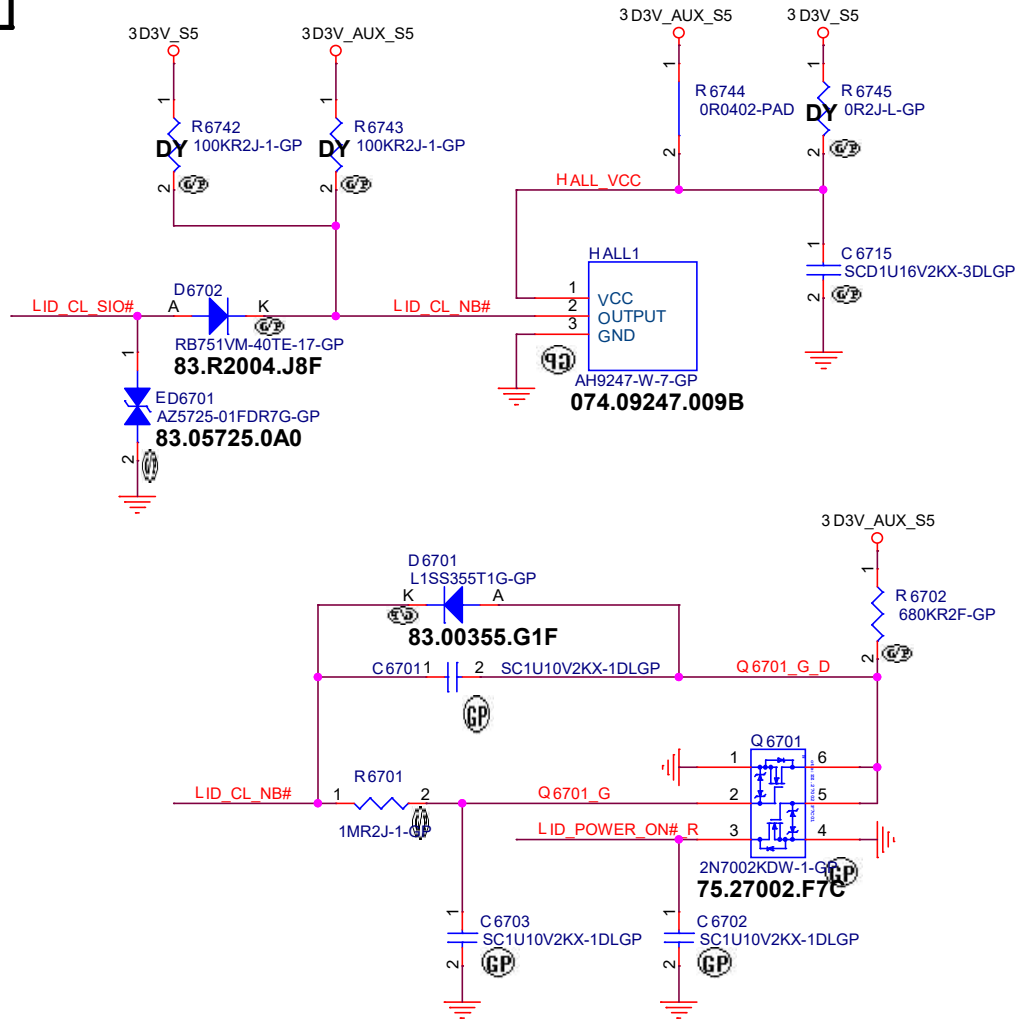
Date: Thursday, March 07, 2019 | Sheet 66 of 106

WWW.AliSaler.Com

# Main Func = HALL SENSOR

24 LID_POWER_ON#_R >>>
20,24,64,92 LID_CL_SIO# <<<

## LID sensor

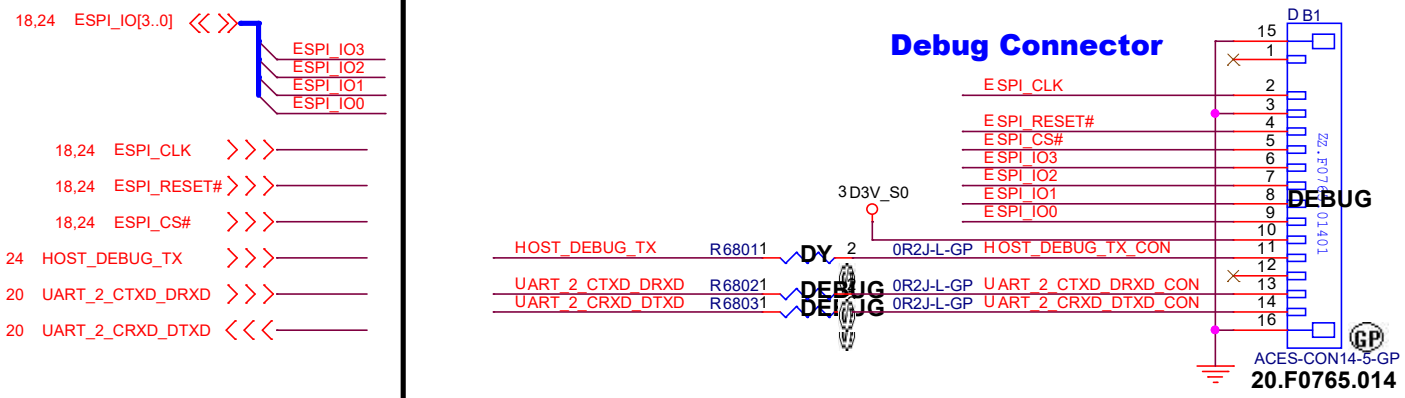



<Core Design>

**Wistron Corporation**
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

| | | |
|---|---|---|
| Title | ***Sensor (Hall-Sensor)*** | |
| Size: A4 | Document Number: ***WASP 13" WHL-U*** | Rev: ***A 00*** |
| Date: Thursday, March 07, 2019 | Sheet 67 of 106 | |

# Main Func = Debug




<Core Design>

**Wistron Corporation**
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Dubug connector*

| Size | Document Number | Rev |
|---|---|---|
| A 4 | *WASP 13" WHL-U* | *A 00* |

Date: Thursday, March 07, 2019 | Sheet 68 of 106

WWW.AliSaler.Com

# (Blanking)

<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

***Reserved***

| Size | Document Number | Rev |
|---|---|---|
| A 4 | ***WASP 13" WHL-U*** | ***A 00*** |

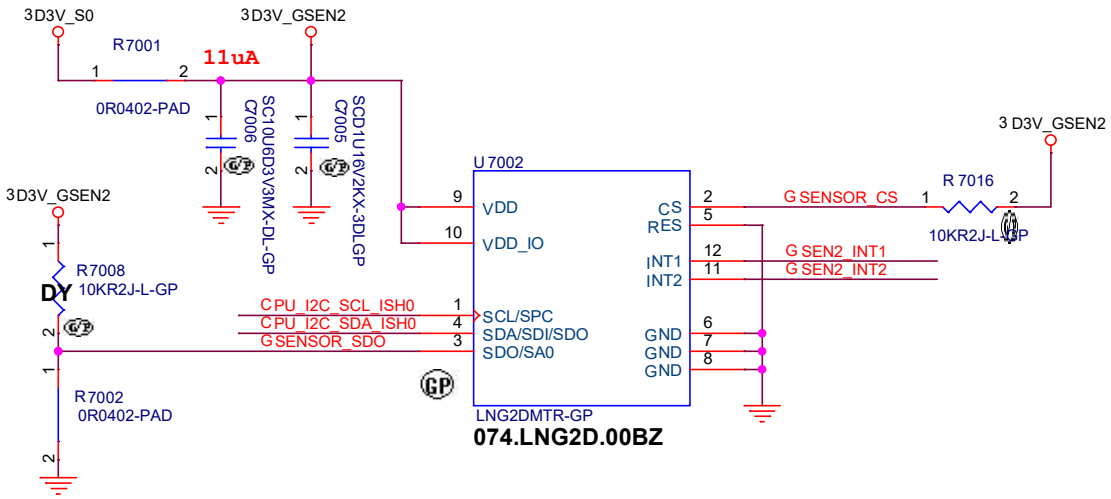
Date: Thursday, March 07, 2019 Sheet 69 o f 106

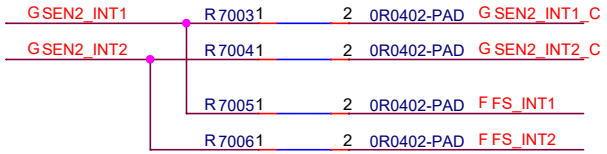
# Main Func = G-sensor

20 GSEN2_INT1_C
20 GSEN2_INT2_C

18 FFS_INT1
20 FFS_INT2

20 CPU_I2C_SCL_ISH0
20 CPU_I2C_SDA_ISH0




<Core Design>

**Wistron Corporation**
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Sensor**

| Size | Document Number | Rev |
|---|---|---|
| A 4 | WASP 13" WHL-U | A 00 |

Date: Thursday, March 07, 2019 Sheet 70 of 106

WWW.AliSaler.Com

# Main Func = TYPEC MUX

## DisplayPort Source

4 DP2_DDI_TX_P0
4 DP2_DDI_TX_N0
4 DP2_DDI_TX_P1
4 DP2_DDI_TX_N1
4 DP2_DDI_TX_P2
4 DP2_DDI_TX_N2
4 DP2_DDI_TX_P3
4 DP2_DDI_TX_N3

## DisplayPort

4,72 DP1_HPD_CPU

4 DP2_AUX_CPU_P
4 DP2_AUX_CPU_N

## USB HOST

16 USB4_USB30_RX_P
16 USB4_USB30_RX_N

16 USB4_USB30_TX_P
16 USB4_USB30_TX_N

## USB3.0 TYPEC CONNECTOR

73 USB1_SBU1
73 USB1_SBU2

73 USB1_SSTX_CON_N1
73 USB1_SSTX_CON_P1

73 USB1_SSTX_CON_N2
73 USB1_SSTX_CON_P2

73 USB1_SSRX_CON_N1
73 USB1_SSRX_CON_P1

73 USB1_SSRX_CON_N2
73 USB1_SSRX_CON_P2

73 USB1_SSRX_MUX_N1
73 USB1_SSRX_MUX_P1

73 USB1_SSRX_MUX_N2
73 USB1_SSRX_MUX_P2

## I2C TO PD

72 I2C_CLK_PD
72 I2C_DATA_PD

3D3V_MUX
R7121 DY 4K7R2J-L-GP HPDIN
R7118 DY 10KR2J-L-GP CAD_SNK
R7101 100KR2J-1-GP DP2_AUX_C_N
R7102 100KR2J-1-GP DP2_AUX_C_P

3D3V_S5 R7124 3D3V_MUX
0R0402-PAD
SC10U6D3V3MX-DL-GP
C7119 C7115 C7116 C7117 C7118
SCD1U25V2KX-1-DL-GP

3D3V_MUX
VCC max. 3.3V/200mA (660mW)
U7101
VCC VCC VCC VCC
DP0P DP0N DP1P DP1N DP2P DP2N DP3P DP3N
RX1P RX1N RX2P RX2N
TX1P TX1N TX2P TX2N
SSRXP SSRXN
SSTXP SSTXN
EQ0 EQ1
HPDIN/DCI_CLK CAD_SNK/DCI_DAT
I2C_EN
SBU1 SBU2
AUXP AUXN
DPEQ0/A1 DPEQ1
SSEQ0/A0 SSEQ1
FLIP/SCL
CTL0/SDA CTL1/HPDIN
GND
TUSB546-DCIRNQR-1-GP
071.00546.M001

DisplayPort Source
DP2_DDI_TX_P0 C7112 SCD1U16V2KX-3DLGP DP2_DDI_TX_C_P0
DP2_DDI_TX_N0 C7113 SCD1U16V2KX-3DLGP DP2_DDI_TX_C_N0
DP2_DDI_TX_P1 C7114 SCD1U16V2KX-3DLGP DP2_DDI_TX_C_P1
DP2_DDI_TX_N1 C7107 SCD1U16V2KX-3DLGP DP2_DDI_TX_C_N1
DP2_DDI_TX_P2 C7109 SCD1U16V2KX-3DLGP DP2_DDI_TX_C_P2
DP2_DDI_TX_N2 C7108 SCD1U16V2KX-3DLGP DP2_DDI_TX_C_N2
DP2_DDI_TX_P3 C7111 SCD1U16V2KX-3DLGP DP2_DDI_TX_C_P3
DP2_DDI_TX_N3 C7110 SCD1U16V2KX-3DLGP DP2_DDI_TX_C_N3

USB1_SSRX_MUX_P1 USB1_SSRX_MUX_N1 USB1_SSRX_MUX_P2 USB1_SSRX_MUX_N2
USB1_SSTX_MUX_P1 USB1_SSTX_MUX_N1 USB1_SSTX_MUX_P2 USB1_SSTX_MUX_N2

USB HOST
USB4_USB30_RX_P C7105 SCD1U16V2KX-3DLGP USB4_USB30_RX_C_P
USB4_USB30_RX_N C7106 SCD1U16V2KX-3DLGP USB4_USB30_RX_C_N
USB4_USB30_TX_P C7103 SCD1U16V2KX-3DLGP USB4_USB30_TX_C_P
USB4_USB30_TX_N C7104 SCD1U16V2KX-3DLGP USB4_USB30_TX_C_N

USB1_SBU1 R7153 0R0402-PAD
USB1_SBU2 R7151 0R0402-PAD
DP2_AUX_C_P C7101 SCD1U25V2KX-1-DL-GP DP2_AUX_CPU_P
DP2_AUX_C_N C7102 SCD1U25V2KX-1-DL-GP DP2_AUX_CPU_N
DPEQ0_A1
DPEQ1
SSEQ0_A0
SSEQ1
I2C_CLK_PD_MUX R7114 0R0402-PAD I2C_CLK_PD
I2C_DATA_PD_MUX R7116 0R0402-PAD I2C_DATA_PD
MUX_HPD_CON R7149 0R0402-PAD DP1_HPD_CPU

Need to BOM change cap power rating to 25V
USB1_SSTX_MUX_P1 C7164 SCD1U25V2KX-1-DL-GP USB1_SSTX_CON_P1
USB1_SSTX_MUX_N1 C7163 SCD1U25V2KX-1-DL-GP USB1_SSTX_CON_N1
USB1_SSRX_MUX_P1 C7120 SCD33U6D3V1MX-GP USB1_SSRX_CON_P1
USB1_SSRX_MUX_N1 C7121 SCD33U6D3V1MX-GP USB1_SSRX_CON_N1
Manual
R7119 220KR2F-L-GP
R7120 220KR2F-L-GP

Need to BOM change cap power rating to 25V
USB1_SSTX_MUX_P2 C7161 SCD1U25V2KX-1-DL-GP USB1_SSTX_CON_P2
USB1_SSTX_MUX_N2 C7162 SCD1U25V2KX-1-DL-GP USB1_SSTX_CON_N2
USB1_SSRX_MUX_P2 C7122 SCD33U6D3V1MX-GP USB1_SSRX_CON_P2
USB1_SSRX_MUX_N2 C7123 SCD33U6D3V1MX-GP USB1_SSRX_CON_N2
Manual
R7123 220KR2F-L-GP
R7122 220KR2F-L-GP

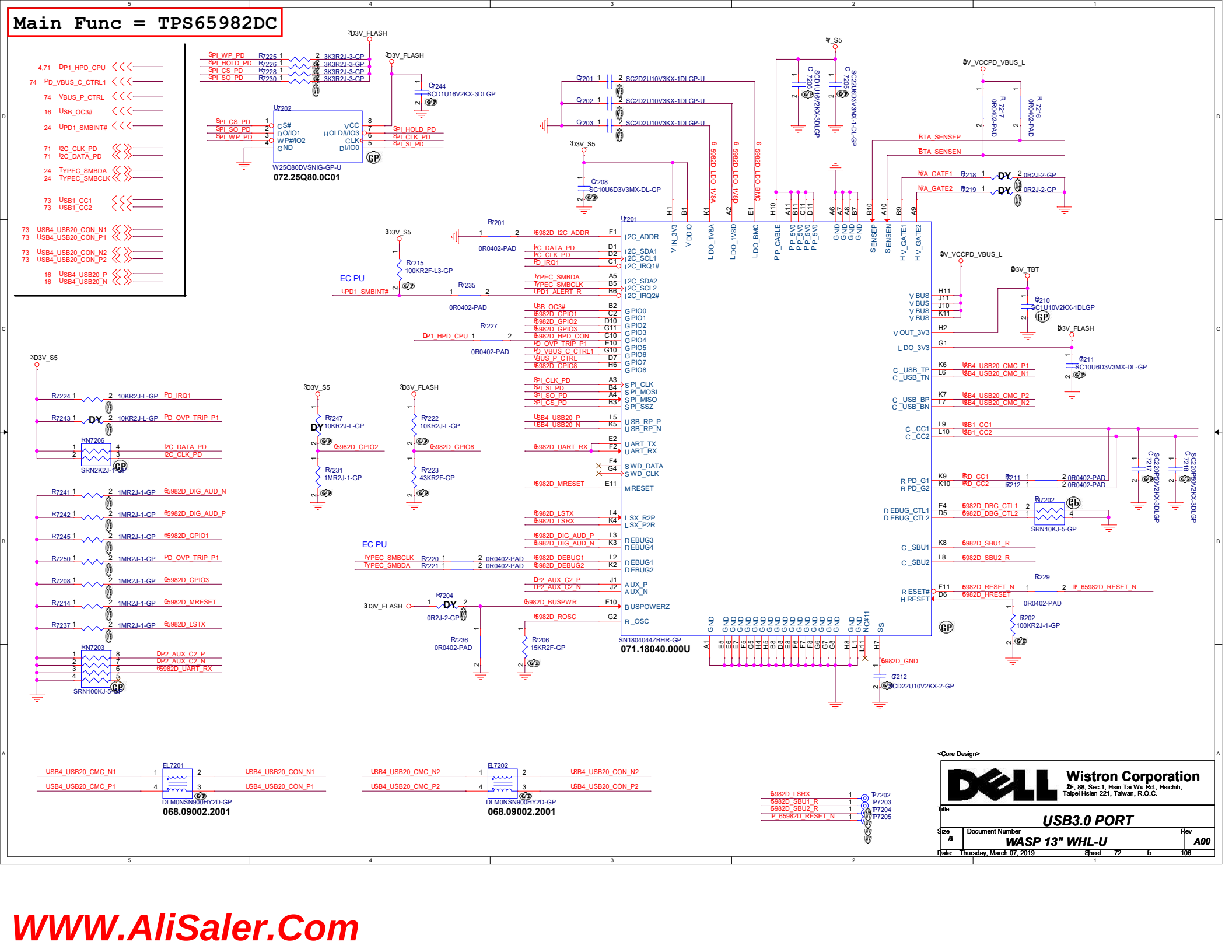
3D3V_MUX
EQ0 R7142 DY 1KR2J-1-GP R7143 1KR2J-1-GP
EQ1 R7140 DY 1KR2J-1-GP R7141 1KR2J-1-GP
I2CEN R7174 1KR2J-1-GP R7173 DY 1KR2J-1-GP
DPEQ1 R7147 DY 1KR2J-1-GP R7170 1KR2J-1-GP
DPEQ0_A1 R7171 DY 1KR2J-1-GP R7172 1KR2J-1-GP
SSEQ1 R7152 DY 1KR2J-1-GP R7144 1KR2J-1-GP
SSEQ0_A0 R7145 DY 1KR2J-1-GP R7146 1KR2J-1-GP

<Core Design>

Wistron Corporation
2F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Type-C MUX
Size: Custom
Document Number: WASP 13" WHL-U
Rev: A 00
Date: Thursday, March 07, 2019
Sheet 71 of 106

# Main Func = TPS65982DC




WWW.AliSaler.Com

# Main Func = TYPEC CONNECTOR

71 USB1_SSRX_MUX_N1
71 USB1_SSRX_MUX_P1
71 USB1_SSRX_MUX_N2
71 USB1_SSRX_MUX_P2
71 USB1_SSRX_CON_N1
71 USB1_SSRX_CON_P1
71 USB1_SSRX_CON_N2
71 USB1_SSRX_CON_P2
71 USB1_SSTX_CON_N1
71 USB1_SSTX_CON_P1
71 USB1_SSTX_CON_N2
71 USB1_SSTX_CON_P2
72 USB4_USB20_CON_N1
72 USB4_USB20_CON_P1
72 USB4_USB20_CON_N2
72 USB4_USB20_CON_P2
71 USB1_SBU1
71 USB1_SBU2
72 USB1_CC1
72 USB1_CC2

USB1_SBU1
USB1_SBU2
R7330 2MR2F-GP
R7331 2MR2F-GP

20V_VCCPD_VBUS_L
20V_VCCPD_VBUS
ER7301 0R5J-5-GP
ER7302 0R5J-5-GP
C7301 SC1U25V3KX-1-DLGP
D7301 BX310F-R1-00000-GP
83.3R010.C8M
DY
C7305 SC10U25V5KX-DL-GP
C7306 SC1U25V3KX-1-DLGP
C7302 SCD1U25V2KX-1-DL-GP
C7303 SCD1U25V2KX-1-DL-GP
C7304 SCD1U25V2KX-1-DL-GP
C7307 SCD1U25V2KX-1-DL-GP

ED7301
USB1_SSTX_CON_N1
USB1_SSTX_CON_P1
USB1_SSRX_MUX_N1
USB1_SSRX_MUX_P1
L05ESDL5V0NA-4-GP
075.00550.0071

ED7302
USB1_SSRX_MUX_P2
USB1_SSRX_MUX_N2
USB1_SSTX_CON_P2
USB1_SSTX_CON_N2
L05ESDL5V0NA-4-GP
075.00550.0071

ED7303
USB4_USB20_CON_N1
USB4_USB20_CON_P1
USB4_USB20_CON_N2
USB4_USB20_CON_P2
L05ESDL5V0NA-4-GP
075.00550.0071

ED7304
USB1_CC1
USB1_CC2
USB1_SBU1
USB1_SBU2
L05ESDL5V0NA-4-GP
075.00550.0071

20V_VCCPD_VBUS
USB1
GND SSTXP1 SSTXN1 VBUS#A4 CC1 DP1 DN1 RFU1 VBUS#A9 SSRXN2 SSRXP2 GND
GND SSTXP2 SSTXN2 VBUS#B4 CC2 DP2 DN2 RFU2 VBUS#B9 SSRXN1 SSRXP1 GND
NP1 NP2
GROUND CHASSIS#13 CHASSIS#14 CHASSIS#15 CHASSIS#20 CHASSIS#21 CHASSIS#22
USB1_SSTX_CON_P1
USB1_SSTX_CON_N1
USB1_CC1
USB4_USB20_CON_P1
USB4_USB20_CON_N1
USB1_SBU1
USB1_SSRX_CON_N2
USB1_SSRX_CON_P2
USB1_SSTX_CON_P2
USB1_SSTX_CON_N2
USB1_CC2
USB4_USB20_CON_P2
USB4_USB20_CON_N2
USB1_SBU2
USB1_SSRX_CON_N1
USB1_SSRX_CON_P1
SKT-USB34-21-GP-U1
022.10005.M021

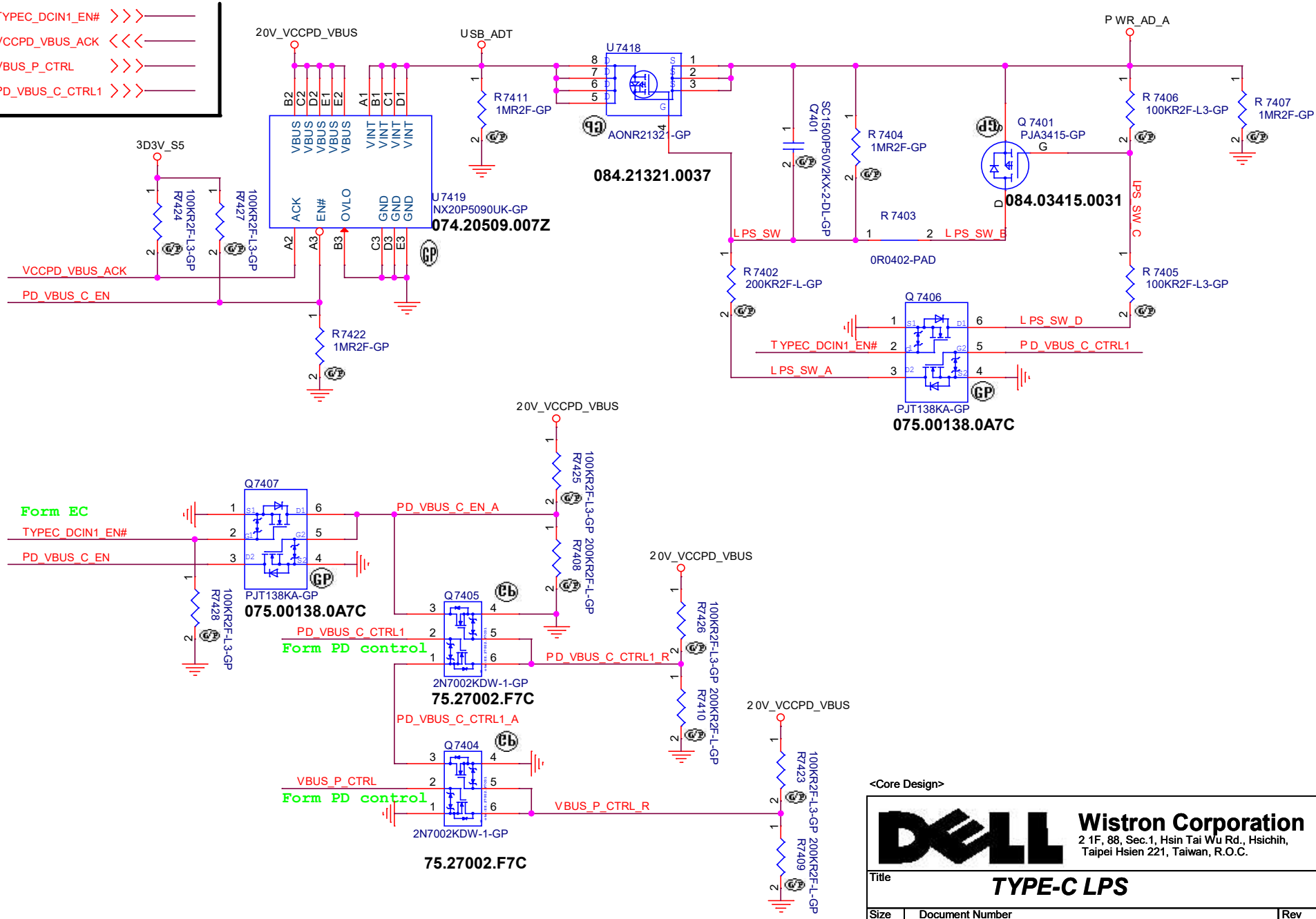
<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU(1/5)PEG
Size: A 4
Document Number: WASP 13" WHL-U
Rev: A00
Date: Thursday, March 07, 2019
Sheet 73 of 106

# Main Func = TYPEC protect

24 TYPEC_DCIN1_EN#
44 VCCPD_VBUS_ACK
72 VBUS_P_CTRL
72 PD_VBUS_C_CTRL1




<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TYPE-C LPS

| Size | Document Number | Rev |
|---|---|---|
| A 4 | WASP 13" WHL-U | A00 |
| Date: Thursday, March 07, 2019 | Sheet 74 of 106 | |

WWW.AliSaler.Com

# (Blanking)

<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
*GPU(3/5)VRAMI/F*

| Size | Document Number | Rev |
|---|---|---|
| A 4 | WASP 13" WHL-U | A00 |

Date: Thursday, March 07, 2019 Sheet 75 o f 106

**Main Func = dGPU**

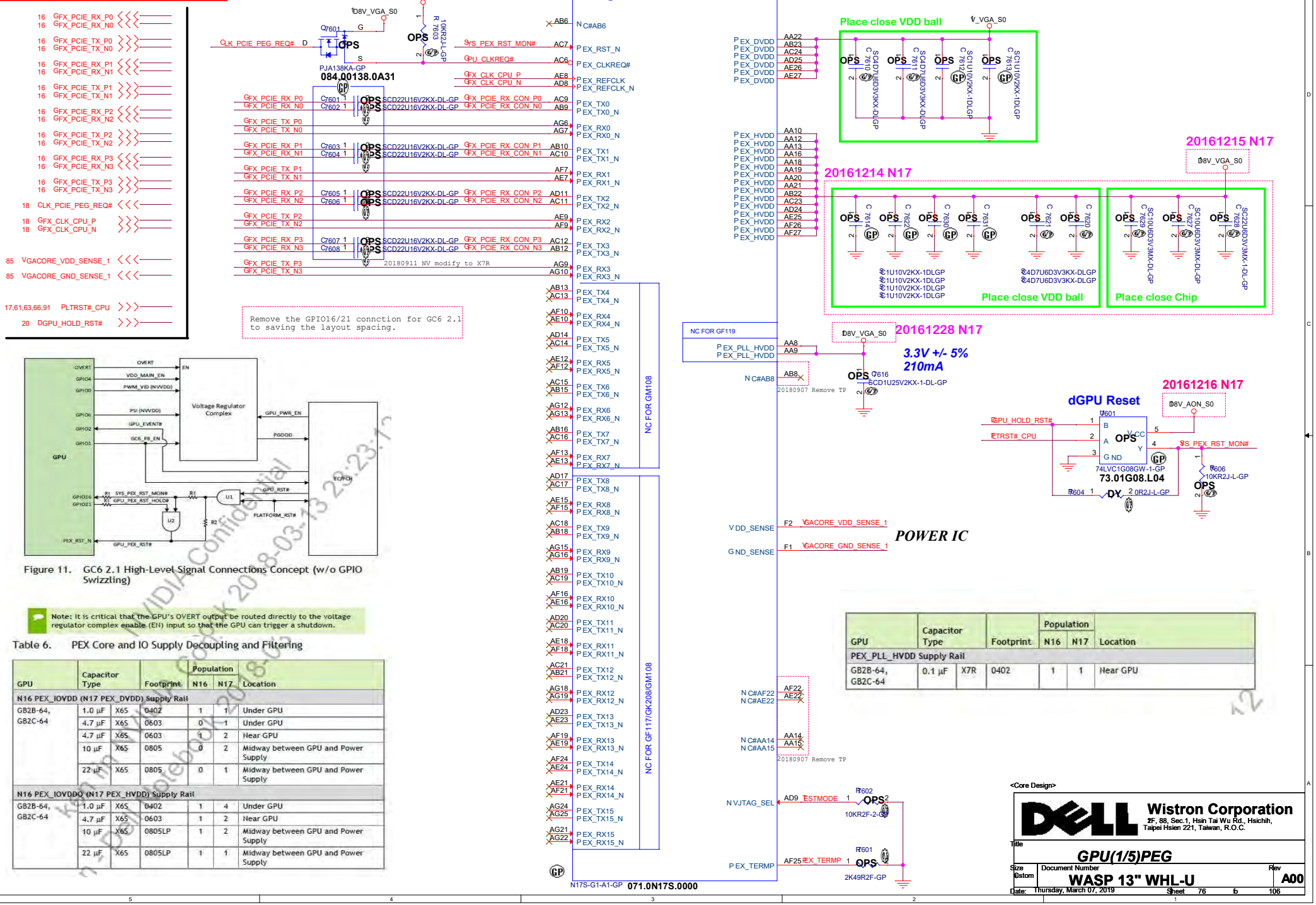



Figure 11. GC6 2.1 High-Level Signal Connections Concept (w/o GPIO Swizzling)

Note: It is critical that the GPU's OVERT output be routed directly to the voltage regulator complex enable (EN) input so that the GPU can trigger a shutdown.

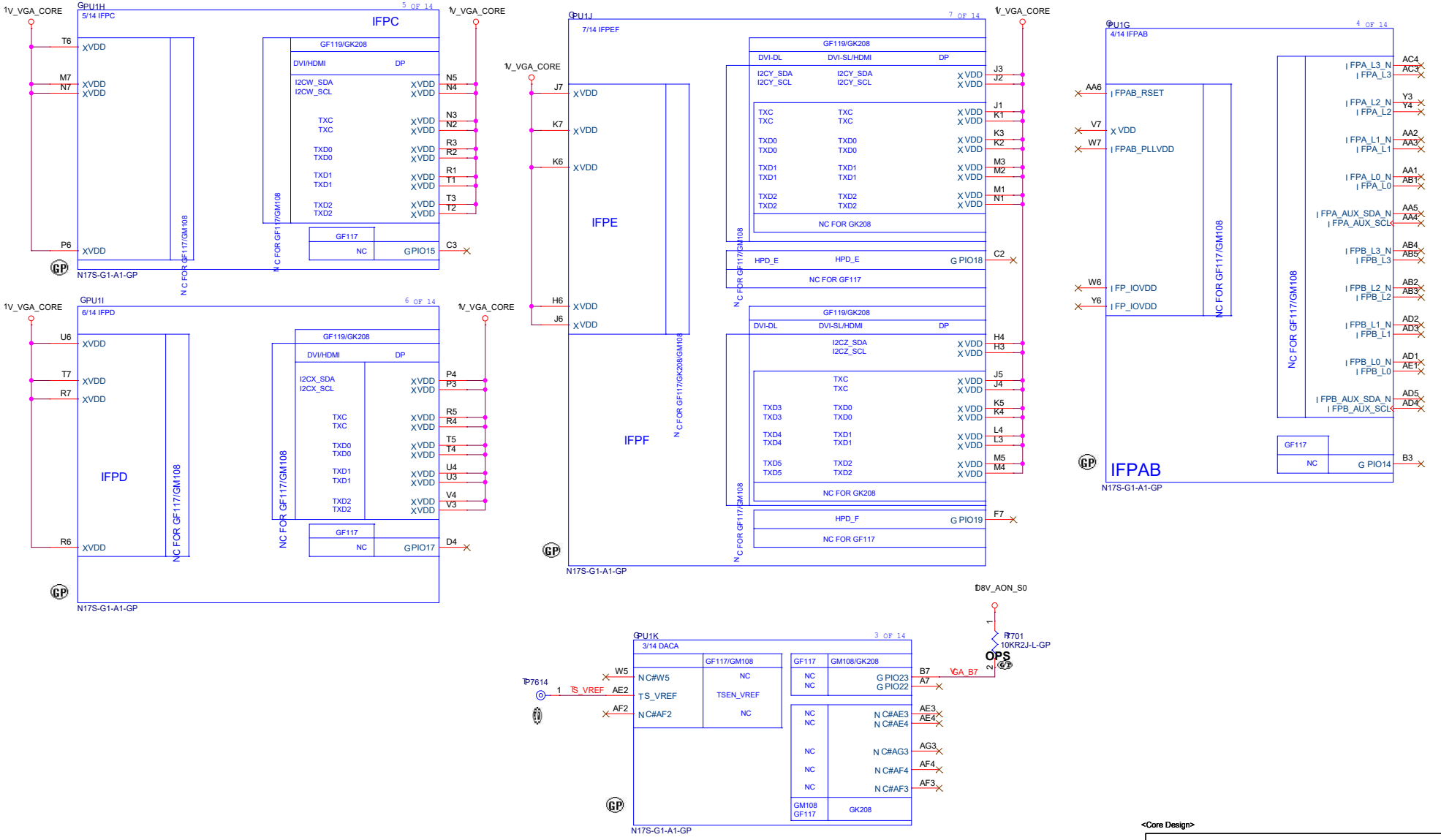
Table 6. PEX Core and IO Supply Decoupling and Filtering

| GPU | Capacitor Type | | Footprint | Population N16 | Population N17 | Location |
|---|---|---|---|---|---|---|
| **N16 PEX_IOVDD (N17 PEX_DVDD) Supply Rail** | | | | | | |
| GB2B-64, GB2C-64 | 1.0 µF | X6S | 0402 | 1 | 1 | Under GPU |
| | 4.7 µF | X6S | 0603 | 0 | 1 | Under GPU |
| | 4.7 µF | X6S | 0603 | 1 | 2 | Near GPU |
| | 10 µF | X6S | 0805 | 0 | 2 | Midway between GPU and Power Supply |
| | 22 µF | X6S | 0805 | 0 | 1 | Midway between GPU and Power Supply |
| **N16 PEX_IOVDDQ (N17 PEX_HVDD) Supply Rail** | | | | | | |
| GB2B-64, GB2C-64 | 1.0 µF | X6S | 0402 | 1 | 4 | Under GPU |
| | 4.7 µF | X6S | 0603 | 1 | 2 | Near GPU |
| | 10 µF | X6S | 0805LP | 1 | 2 | Midway between GPU and Power Supply |
| | 22 µF | X6S | 0805LP | 1 | 1 | Midway between GPU and Power Supply |

| GPU | Capacitor Type | | Footprint | Population N16 | Population N17 | Location |
|---|---|---|---|---|---|---|
| **PEX_PLL_HVDD Supply Rail** | | | | | | |
| GB2B-64, GB2C-64 | 0.1 µF | X7R | 0402 | 1 | 1 | Near GPU |

WWW.AliSaler.Com

# Main Func = dGPU




<Core Design>

Wistron Corporation
2F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU(2/5)DIGITALOUT

| Size | Document Number | Rev |
|---|---|---|
| B | WASP 13" WHL-U | A00 |

Date: Thursday, March 07, 2019 Sheet 77 of 106

# Main Func = dGPU

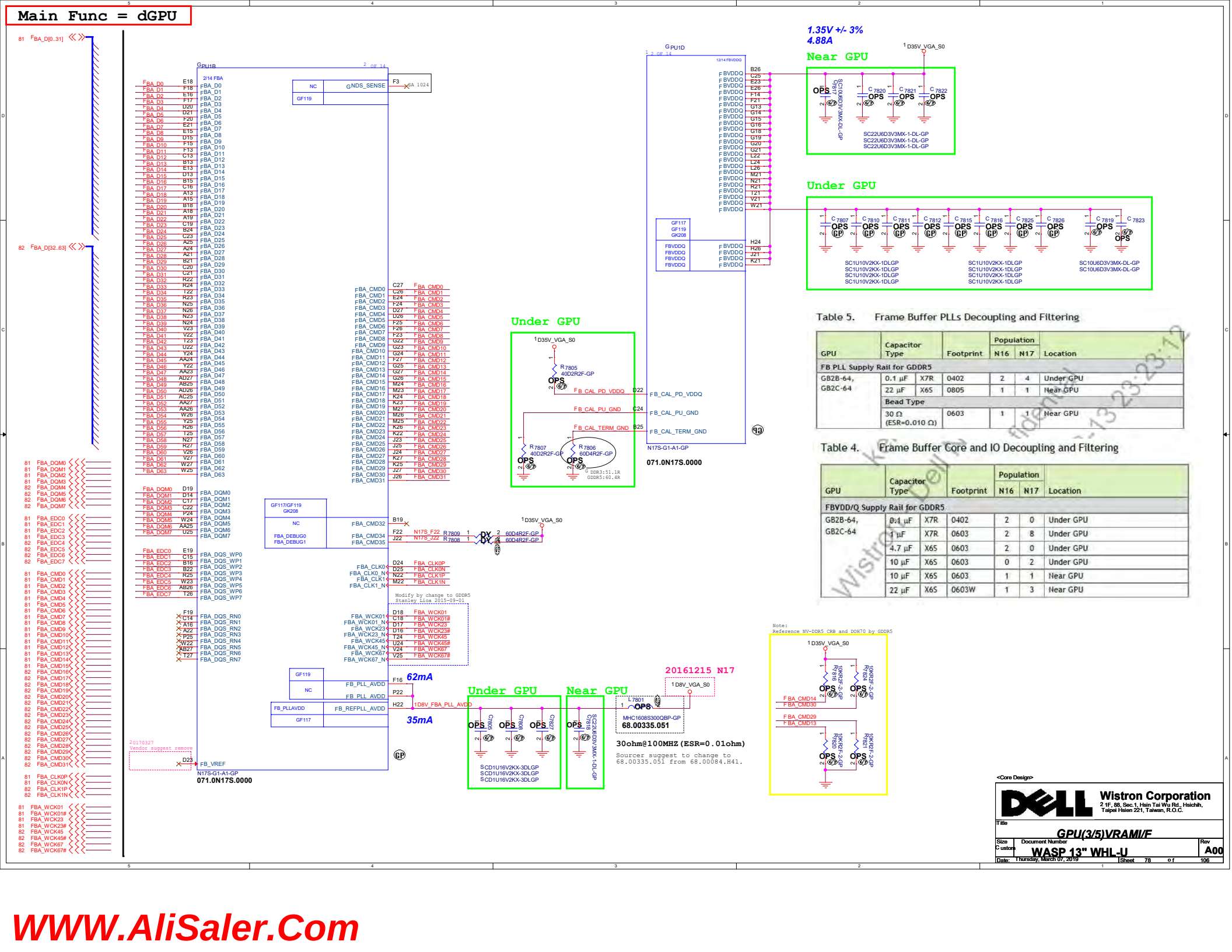



Table 5. Frame Buffer PLLs Decoupling and Filtering

| GPU | Capacitor Type | | Footprint | Population N16 | Population N17 | Location |
|---|---|---|---|---|---|---|
| FB PLL Supply Rail for GDDR5 | | | | | | |
| GB2B-64, GB2C-64 | 0.1 µF | X7R | 0402 | 2 | 4 | Under GPU |
| | 22 µF | X6S | 0805 | 1 | 1 | Near GPU |
| | Bead Type | | | | | |
| | 30 Ω (ESR=0.010 Ω) | | 0603 | 1 | 1 | Near GPU |

Table 4. Frame Buffer Core and IO Decoupling and Filtering

| GPU | Capacitor Type | | Footprint | Population N16 | Population N17 | Location |
|---|---|---|---|---|---|---|
| FBVDD/Q Supply Rail for GDDR5 | | | | | | |
| GB2B-64, GB2C-64 | 0.1 µF | X7R | 0402 | 2 | 0 | Under GPU |
| | 1 µF | X7R | 0603 | 2 | 8 | Under GPU |
| | 4.7 µF | X6S | 0603 | 2 | 0 | Under GPU |
| | 10 µF | X6S | 0603 | 0 | 2 | Under GPU |
| | 10 µF | X6S | 0603 | 1 | 1 | Near GPU |
| | 22 µF | X6S | 0603W | 1 | 3 | Near GPU |

Note: Reference NV-DDR5 CRB and DOH70 by GDDR5

<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

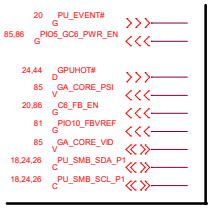
Title: GPU(3/5)VRAMI/F

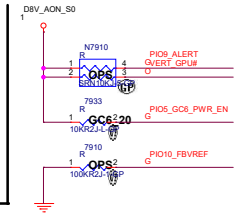
Size: C | Document Number: WASP 13" WHL-U | Rev: A00

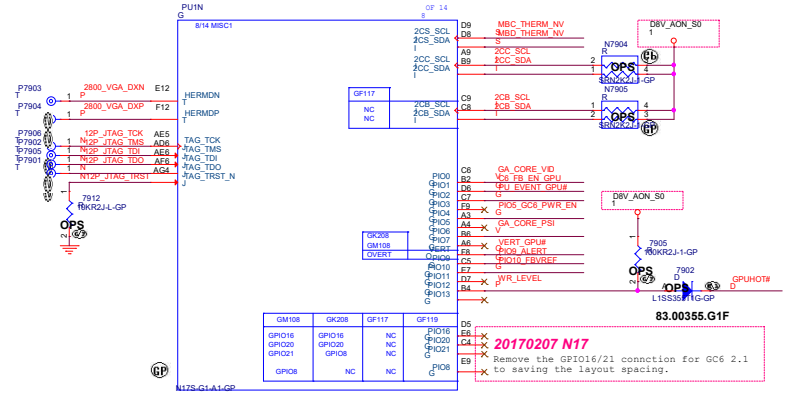
Date: Thursday, March 07, 2019 | Sheet 78 of 106

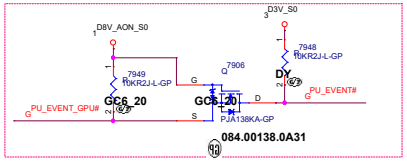
WWW.AliSaler.Com

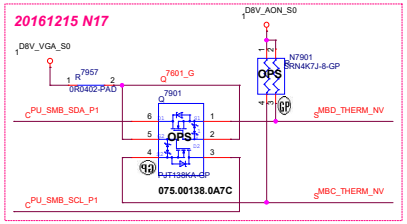
# Main Func = dGPU

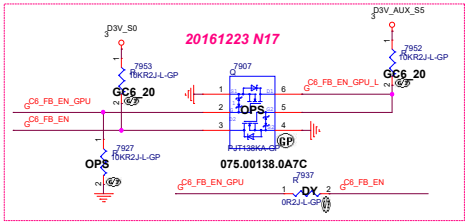


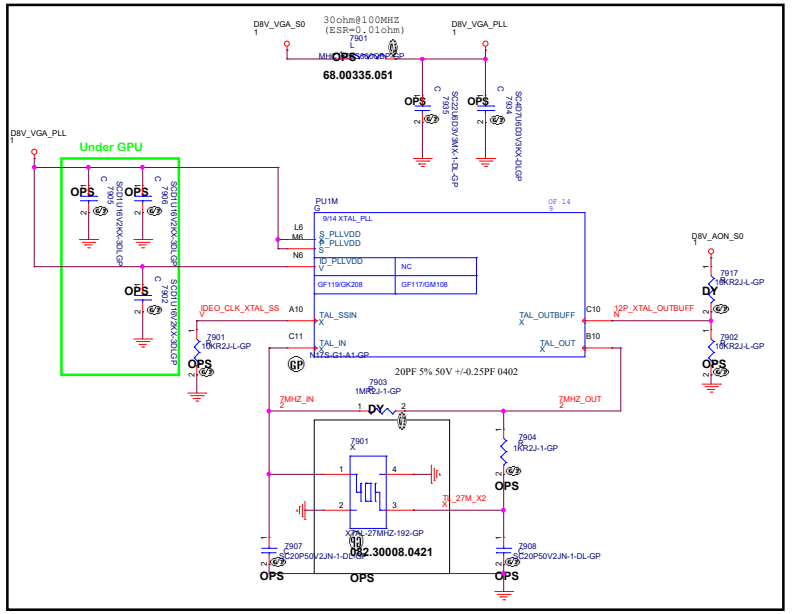



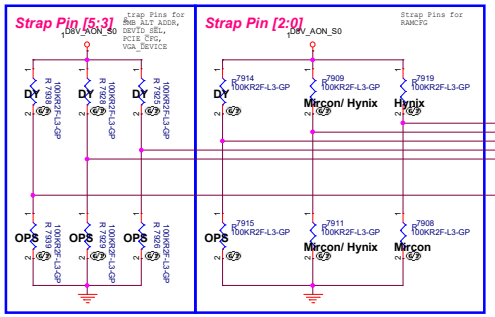




15V-GS supports Binary Mode.
N16V-GM supports Multi-Level Strap.







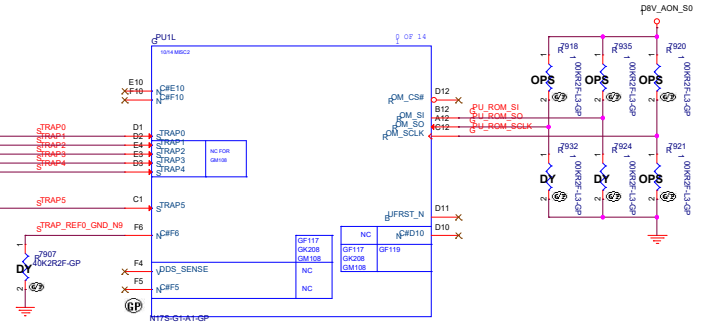



Table 5.5 SORx_EXPOSED Strap Enablement for Down Designs

| Row Index | Strap Pins (see Note) | | | Resulting SORx_EXPOSED Enablements | | | |
|---|---|---|---|---|---|---|---|
| | ROM_SO | ROM_SI | ROM_SCLK | SOR3_EXPOSED | SOR2_EXPOSED | SOR1_EXPOSED | SOR0_EXPOSED |
| 15 | L | L | L | ENABLED | ENABLED | ENABLED | ENABLED |
| 14 | L | L | H | ENABLED | ENABLED | ENABLED | disabled |
| 13 | L | H | L | ENABLED | ENABLED | disabled | ENABLED |
| 12 | L | H | H | ENABLED | ENABLED | disabled | disabled |
| 3 | H | H | L | ENABLED | disabled | disabled | disabled |
| 0 | H | H | H | disabled | disabled | disabled | disabled |
| | M | X | X | (Reserved; do not configure) | | | |
| | All other Strap Configurations | | | (Reserved) | | | |

Table 5.6 SMB ALT_ADDR, DEVTD_SEL, PCIE_CFG, VGA_DEVICE

| Strap Pins (Note 1) | | | Functions Selected by This Strapping | | | |
|---|---|---|---|---|---|---|
| STRAP5 | STRAP4 | STRAP3 | SMB_ALT_ADDR | DEVID_SEL | PCIE_CFG | VGA_DEVICE |
| L | L | L | 0 | 0 | 0 | 0 |
| L | L | H | 0 | 0 | 0 | 1 |
| L | L | M | 0 | 0 | 1 | 0 |
| L | H | L | 0 | 0 | 1 | 1 |
| L | H | H | 0 | 1 | 0 | 0 |
| L | H | M | 0 | 1 | 0 | 1 |
| L | M | L | 0 | 1 | 1 | 0 |
| L | M | H | 0 | 1 | 1 | 1 |
| H | L | L | 1 | 0 | 0 | 0 |
| H | L | H | 1 | 0 | 0 | 1 |
| H | L | M | 1 | 0 | 1 | 0 |
| H | H | L | 1 | 0 | 1 | 1 |
| H | H | H | 1 | 1 | 0 | 0 |
| H | H | M | 1 | 1 | 0 | 1 |
| H | M | L | 1 | 1 | 1 | 0 |
| H | M | H | 1 | 1 | 1 | 1 |
| H | M | M | 1 | 0 | 0 | 0 |
| M | L | L | 1 | 0 | 0 | 1 |
| M | L | H | 1 | 0 | 1 | 0 |

Table 5.3 RAMCFG

| Strap Pins (see Note) | | | RAMCFG Setting Number (see Memory RVL for memory configs corresponding to these numbers) |
|---|---|---|---|
| STRAP2 | STRAP1 | STRAP0 | |
| L | L | L | 0 (0x0000) |
| L | L | H | 1 (0x0001) |
| L | H | L | 2 (0x0002) |
| L | H | H | 3 (0x0003) |
| H | L | L | 4 (0x0004) |
| H | L | H | 5 (0x0005) |
| H | H | L | 6 (0x0006) |
| H | H | H | 7 (0x0007) |
| L | M | L | 8 (0x0008) |
| L | M | H | 9 (0x0009) |
| L | H | M | 10 (0x000A) |
| H | M | L | 11 (0x000B) |
| H | M | H | 12 (0x000C) |
| H | L | M | 13 (0x000D) |

Table 5. N17S-G0/G2 GDDR5 Recommended Memories

| Memory Density | Allowed Memory Configuration | FBVDD/Q | Vendor | Manufacturer Part Number | Die Revision | Strap | Memory Speed Grade | Date Code Alert | Qual Plan | Status |
|---|---|---|---|---|---|---|---|---|---|---|
| 8 Gb | 256Mx32 512Mx16 | 1.35V | Micron | MT51J256M32HF-80:B | B-die | 0x9 | 8 Gbps | N/A | Full | Production ready |
| | | | Hynix | H5GC8H24AJR-R2C | A-die | 0xA | 8 Gbps | N/A | Full | Production ready |

Notes:
1. For N17S-G0/G2, the maximum allowable memory case temperature is 85 °C.
2. N17S-G0/G2 running at 3.0 GHz (without intent to run 3.5 GHz at a later stage) can also use the memory configurations in Table 4 for N17S-G1.

Cheng-Yuan Confidential, 2018-08-31

<Core Design>

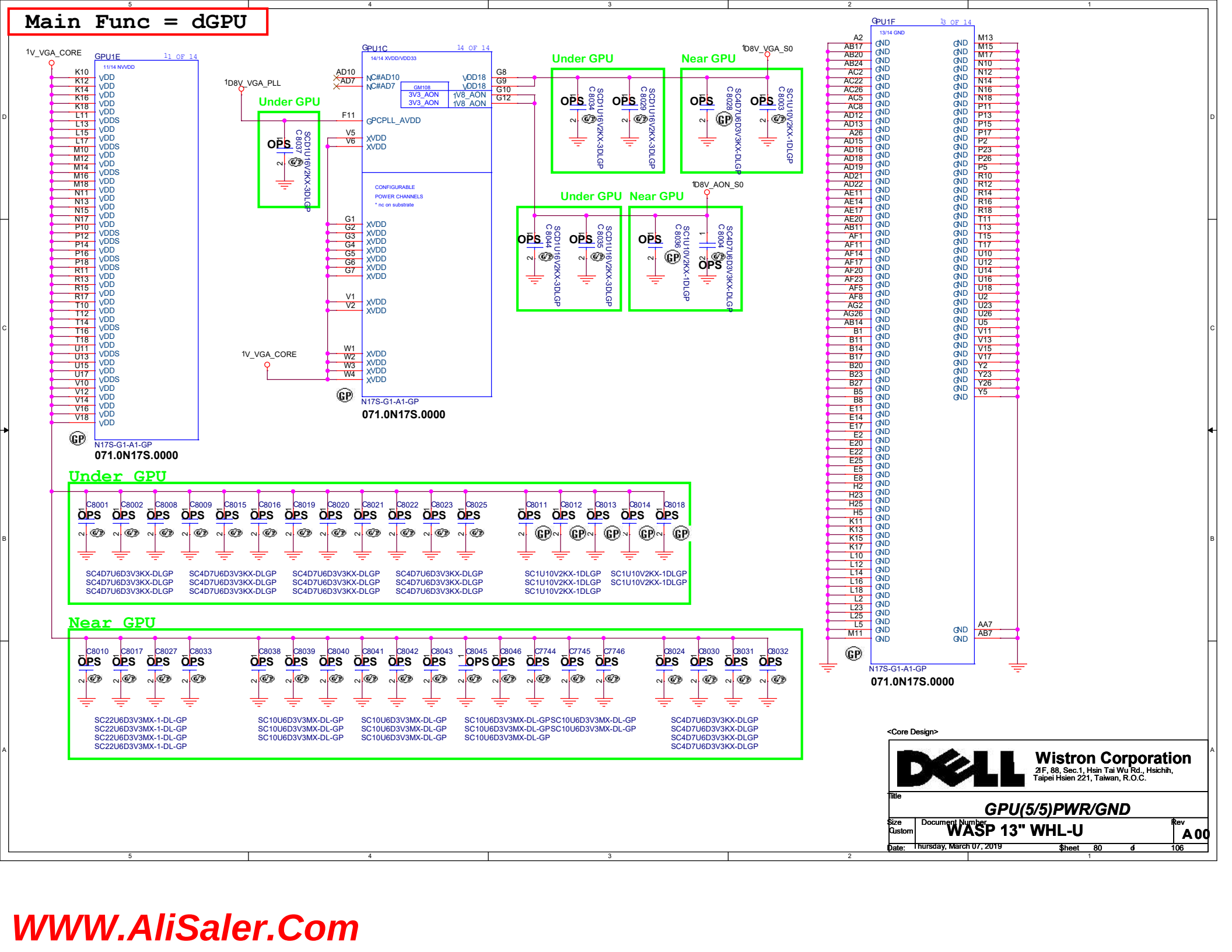
Wistron Corporation
3F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU(4/5)GPIO/STRAP

Size: A | Document Number: WASP 13" WHL-U | Rev: A00

Date: Thursday, March 07, 2019 | Sheet 79 of 108

# Main Func = dGPU




<Core Design>

**Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

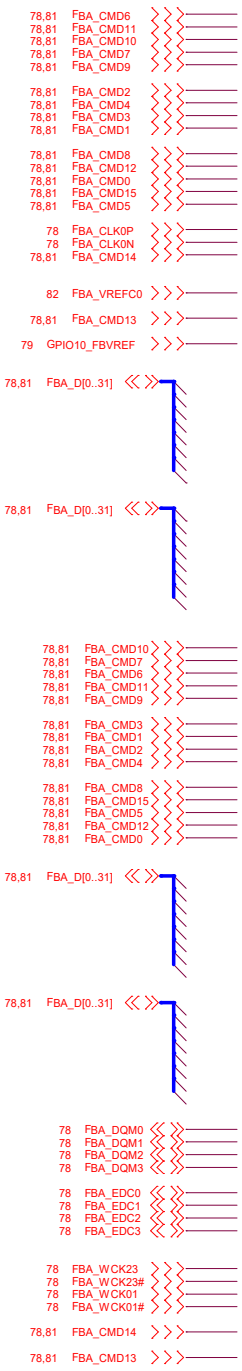
Title: **GPU(5/5)PWR/GND**

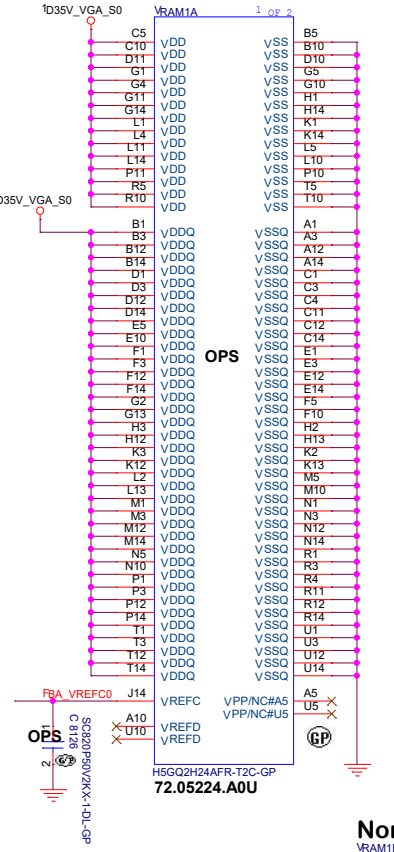
| Size | Document Number | Rev |
|---|---|---|
| Custom | WASP 13" WHL-U | A00 |

Date: Thursday, March 07, 2019 Sheet 80 of 106

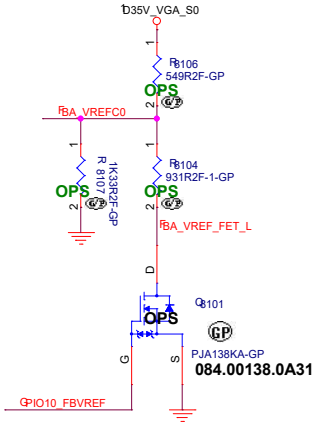
WWW.AliSaler.Com

# SSID = VRAM



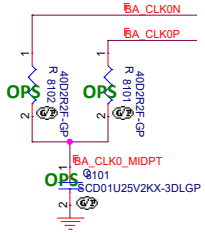




## Frame Buffer Patition A-Lower Half

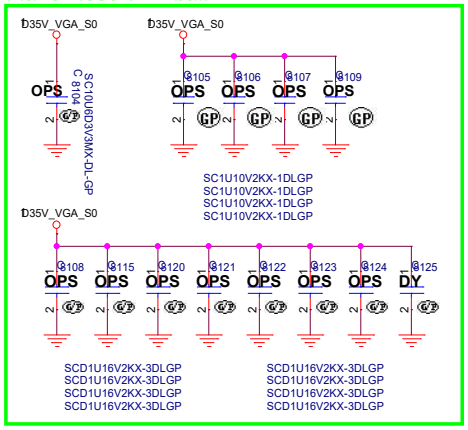



**FBVREF Termination**

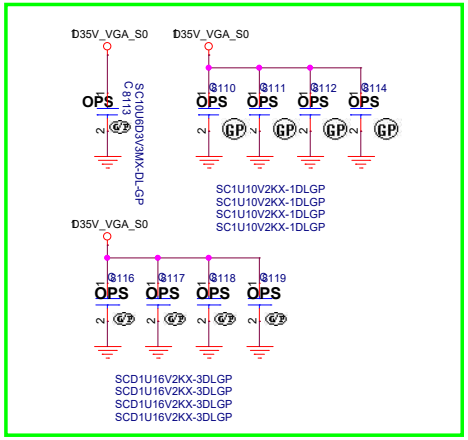
| Type | FBVREF% | Voltage | GPU_GPIO10 |
|---|---|---|---|
| Un-termination | 50% | 0.749V | High |
| Termination | 70% | 1.0617V | Low |



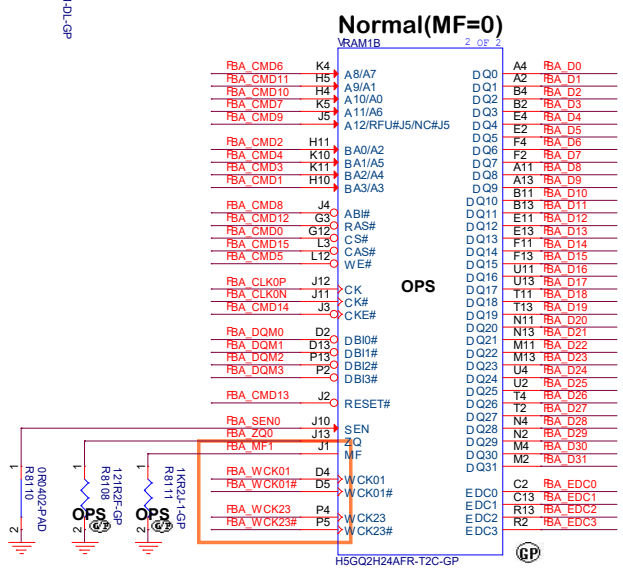

## Place close VDD ball




## Place close VDDQ ball




## Normal(MF=0)







<Core Design>

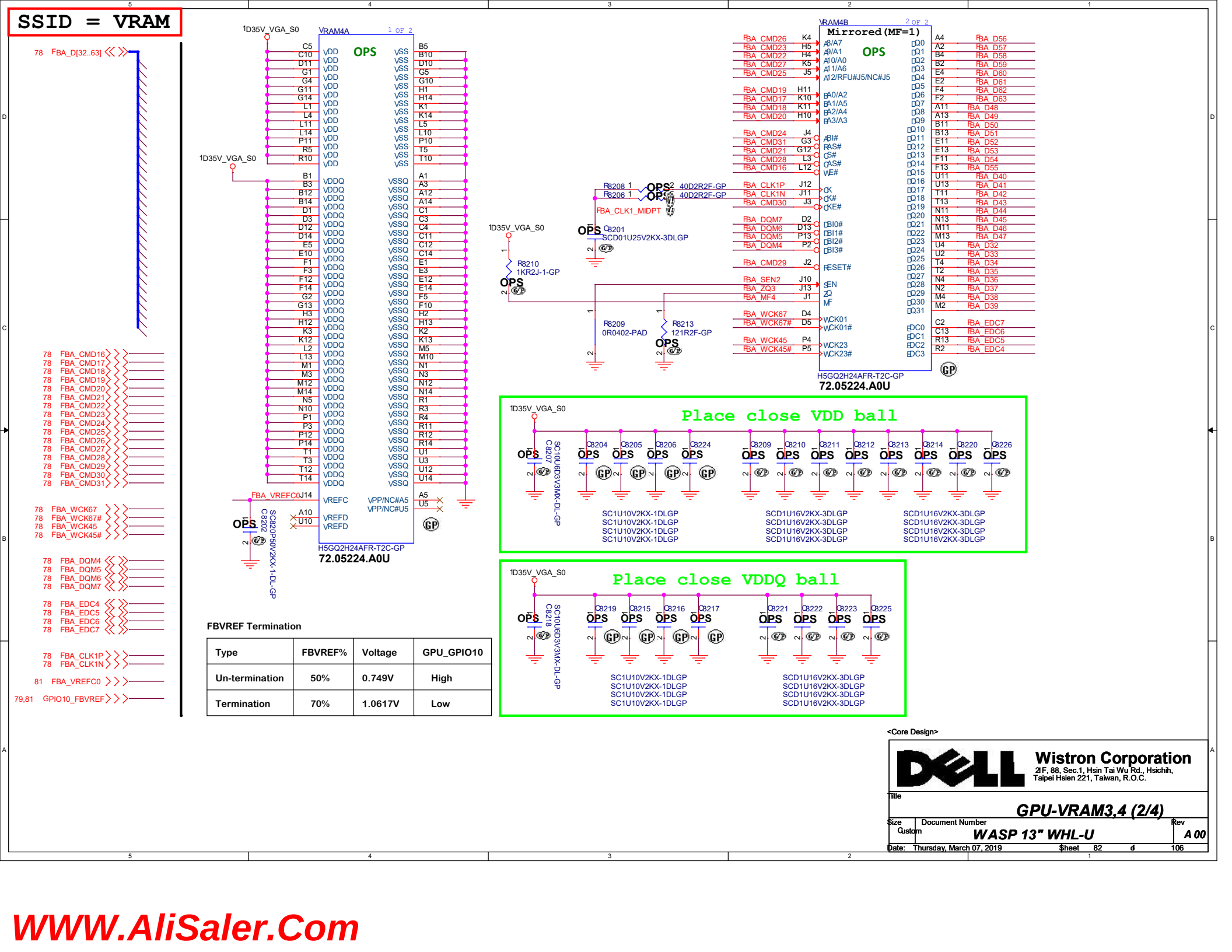
Wistron Corporation
2F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM1,2 (1/4)

Size: A | Document Number: WASP 13" WHL-U | Rev: A00

Date: Thursday, March 07, 2019 | Sheet 81 of 106

# SSID = VRAM




**FBVREF Termination**

| Type | FBVREF% | Voltage | GPU_GPIO10 |
|---|---|---|---|
| Un-termination | 50% | 0.749V | High |
| Termination | 70% | 1.0617V | Low |

<Core Design>

Wistron Corporation
2F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM3,4 (2/4)

Size: Custom | Document Number: WASP 13" WHL-U | Rev: A 00

Date: Thursday, March 07, 2019 | Sheet 82 of 106

WWW.AliSaler.Com

# (Blanking)

<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *GPU-VRAM5,6 (3/4)*

| Size | Document Number | Rev |
|---|---|---|
| A 4 | WASP 13" WHL-U | A00 |

Date: Thursday, March 07, 2019 Sheet 83 o f 106

(Blanking)

<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM7,8 (4/4)

| Size | Document Number | Rev |
|---|---|---|
| A 4 | WASP 13" WHL-U | A00 |

Date: Thursday, March 07, 2019 Sheet 84 o f 106

WWW.AliSaler.Com

OFFPAGE-Signal

OFFPAGE-GAP

# RT8816A For NVVDDS

VGA : N17S-G2 / NVVDD
EDP-Continuous : 28.6A
EDP-Peak : 60.3A

need 1.8V

1. Check EE side
2. Modify DAT

PH on EE side

EE need check

Figure 8.8 GA 2.1 Voltage Regulator Complex Signal Connection

For VGA_CORE sequence
EE need check

Table 1

| Operation Phase Number | PSI Voltage Setting |
|---|---|
| 1phase with DEM | 0V to 0.4V |
| 1phase with CCM | 0.7V to 0.8V |
| 2Phase with DEM | 1.35V to 1.55V |
| 2phase with CCM | 1.6V to 5.5V |

ID:31/54A ,
Rdson: 6.8~8.6/2.8~3.5m (Q1/Q2)

Cyntec 6.8mmx7.3mmx3mm
DCR: 1.9~2.3 mohm
Idc : 27A , Isat : 61A

VGA : N17S-G2 / NVVDD
EDP-Continuous : 28.6A
EDP-Peak : 60.3A

OCP setting

SS setting

Place Near GPU (NVVDDS)
1X330uF (Poscap) - PTB511 (Page85)

| | | | |
|---|---|---|---|
| Core Design | Wistron Corporation | | |
| Title | GPU (RT8816A_VGA) | | |
| Size | Document Number | | Rev |
| A | W ASP 13" WHL-U | | A0 |
| Date: Thursday, March 07, 2013 | Sheet 85 of 106 | | |

Main Func = dGPU

RT5797 for 1.8V_AON_S0

Vo=0.6x(1+R1/R2)
=0.6x(1+100/49.9)
=1.802V

1D8V_AON_S0 to 1D8V_VGA_S0

dGPU Power Discharge Circuit

1V_VGA_S0

1D35V_VGA_S0

Discharge schematic change (solution different)
2010915 Alden chiang modify

VGA_CORE

1D8V_VGA_S0

1D8V_AON_S0

For tuning VGA_CORE sequence.

RT5797 for 1V_VGA_S0

Desigh current = 300mA

Vo=0.6x(1+R1/R2)
=0.6x(1+34.8/51)
=1.009V

1D35V_VGA_S0

SY8288RAC for 1D35V

Cyntec 5 x 5 x 3.0mm
DCR: 13~14mOhm
Idc :7A , Isat : 11A

Design Current=5.6A
OCP=8A

Vo=0.6x(1+R1/R2)
=0.6x(1+15/12)
=1.35V

| OCP setting | |
|---|---|
| High | 16A |
| Float | 12A |
| Low | 8A |

[DG-07158-001 Rev03]

WWW.AliSaler.Com


Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DISCRETE VGA POWER
Size: C (usiim) | Document Number: WASP 13" WHL-U | Rev: A 00
Date: Thursday, March 07, 2019 | Sheet 86 of 106

# (Blanking)

<Core Design>

**Wistron Corporation**
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
***(Reserved)***

| Size | Document Number | Rev |
|---|---|---|
| A 4 | ***WASP 13" WHL-U*** | |

Date: Thursday, March 07, 2019 | Sheet 87 o f 106

(Blanking)

<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Reserved**

| Size | Document Number | Rev |
|---|---|---|
| A 4 | WASP 13" WHL-U | A 00 |

Date: Thursday, March 07, 2019 Sheet 88 o f 106

WWW.AliSaler.Com

# Main Func = UnusedParts

| | | | |
|---|---|---|---|
| H51 STFT237B158R128H48-GP 434.0FD01.0001 | H52 STFT237B158R128H48-GP 434.0FD01.0001 | H5 HOLE233R142-GP-U1 ZZ.00PAD.5S1 | H20 HOLE233R142-GP-U1 ZZ.00PAD.5S1 |
| H9 HOLE233R142-GP-U1 ZZ.00PAD.5S1 | H10 HOLE233R142-GP-U1 ZZ.00PAD.5S1 | H11 HOLE233R142-GP-U1 ZZ.00PAD.5S1 | H12 HOLE233R142-GP-U1 ZZ.00PAD.5S1 |
| H13 HOLE276R150-GP ZZ.00PAD.H91 | H14 HOLE276R150-GP ZZ.00PAD.H91 | H15 HOLE276R150-GP ZZ.00PAD.H91 | H22 HOLET237B213R142-GP ZZ.SCREW.0A1 |

1V_VCCGT
1V_CPU_CORE
1V_VCCSA
5V_S0
19V_DCBATOUT
5V_S5
1D2V_S3
3D3V_S0
1V_VGA_CORE
19V_DCBATOUT
1D0V_S5
3D3V_S5
1V_VGA_CORE
19V_DCBATOUT
PWR_DCBATOUT_VCCSA
PWR_AD_B
1D35V_VGA_S0
1V_CPU_CORE
1V_VCCGT
3D3V_S5
5V_S5
1D2V_S3
PWR_AD_B
1D35V_VGA_S0
1V_CPU_CORE
1V_VCCGT
3D3V_S5
3D3V_S0
1D2V_S3

SC10U25V3MX-5-GP
SC10U25V3MX-5-GP
SC10U25V3MX-5-GP

<Core Design>

Wistron Corporation
2F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: UNUSED PARTS/EMI Capacitors

| Size | Document Number | Rev |
|---|---|---|
| A4 | WASP 13" WHL-U | A00 |

Date: Thursday, March 07, 2019 Sheet 89 of 106

# (Blanking)

<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Reserved**

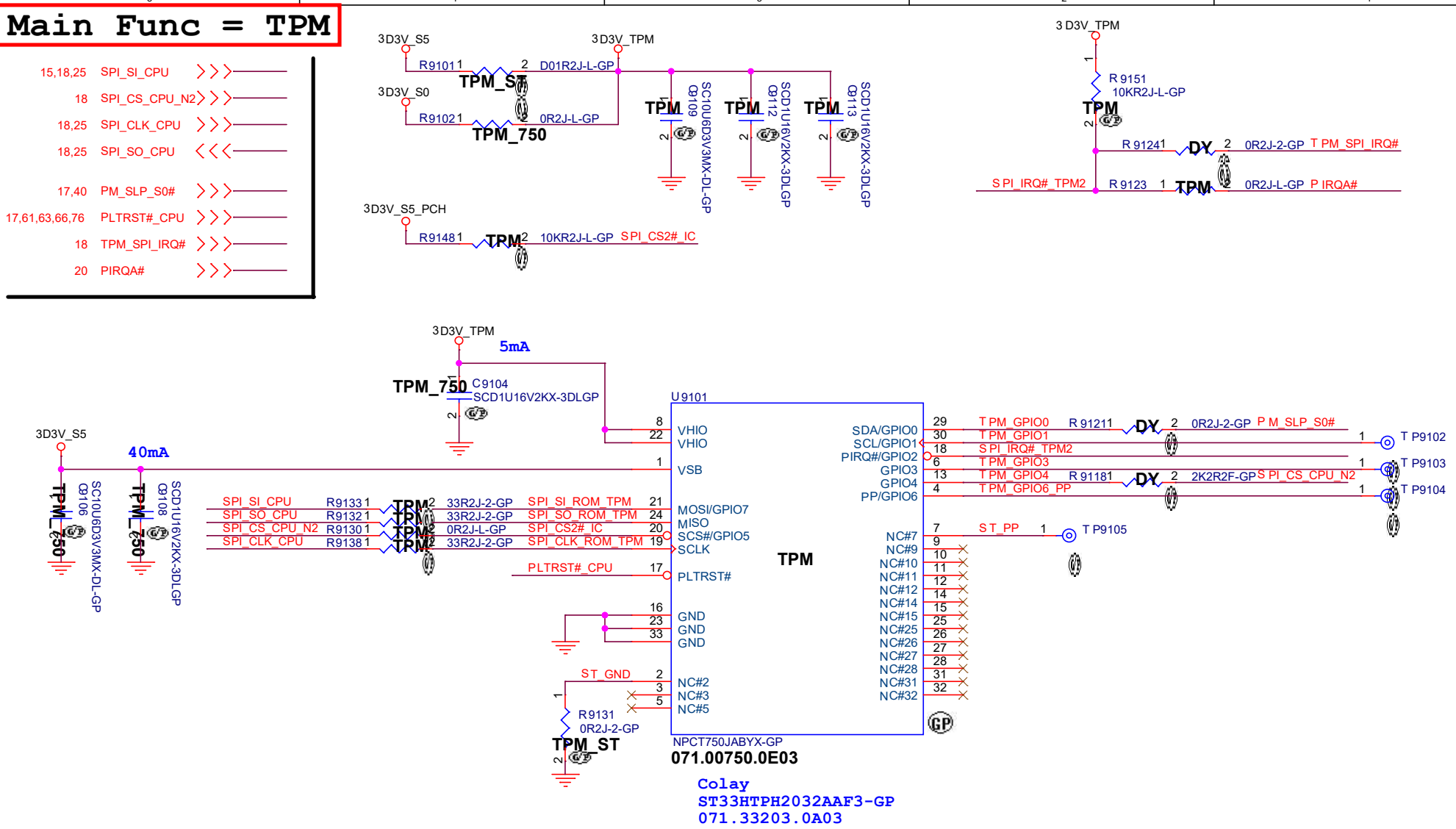
| Size | Document Number | Rev |
|---|---|---|
| A 4 | WASP 13" WHL-U | A 00 |

Date: Thursday, March 07, 2019 Sheet 90 o f 106

WWW.AliSaler.Com

# Main Func = TPM

| | | |
|---|---|---|
| 15,18,25 | SPI_SI_CPU | >> |
| 18 | SPI_CS_CPU_N2 | >> |
| 18,25 | SPI_CLK_CPU | >> |
| 18,25 | SPI_SO_CPU | << |
| 17,40 | PM_SLP_S0# | >> |
| 17,61,63,66,76 | PLTRST#_CPU | >> |
| 18 | TPM_SPI_IRQ# | >> |
| 20 | PIRQA# | >> |




<Core Design>

**Wistron Corporation**
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPM2.0**

| Size | Document Number | Rev |
|---|---|---|
| A 4 | WASP 13" WHL-U | A 00 |

Date: Thursday, March 07, 2019 | Sheet 91 of 106

# Main Func = FPR

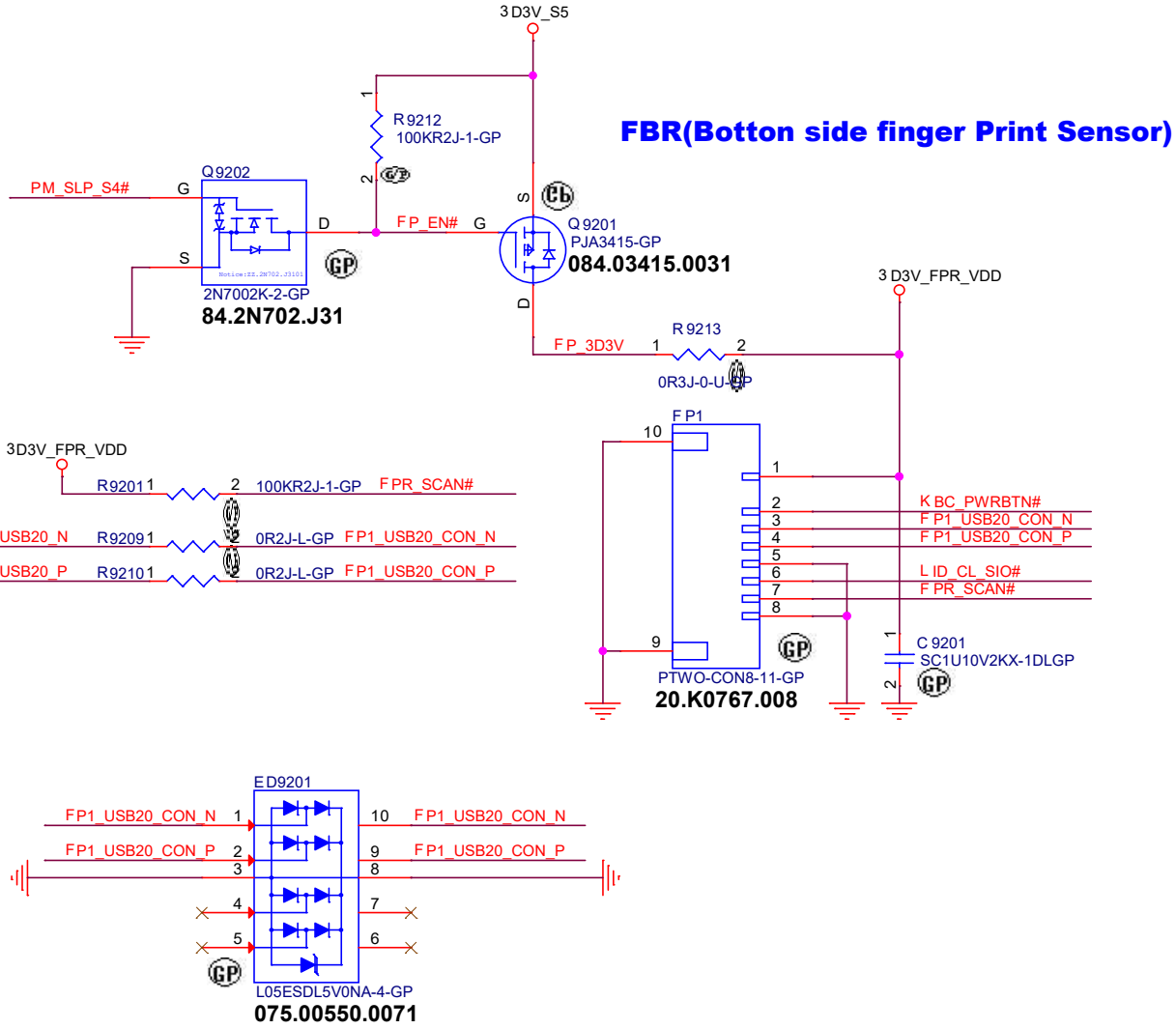
16 FP1_USB20_N
16 FP1_USB20_P
24 FPR_SCAN#
24,64 KBC_PWRBTN#
17,40,51 PM_SLP_S4#
20,24,64,67 LID_CL_SIO#

| | PM_SLP_S4# | FP_3D3V |
|---|---|---|
| S0 | 1 | 1 |
| S3 | 1 | 1 |
| S4 | 0 | 0 |
| S5 | 0 | 0 |

**GF5288WN1+GF128A+GM168 Module design**

**CN PIN Map**

| Pin NO. | INFO |
|---|---|
| 1 | VCC 3.3V |
| 2 | PWBTN |
| 3 | USB N |
| 4 | USB P |
| 5 | GND |
| 6 | LID closed |
| 7 | GPIO Key shielding |
| 8 | GND (ID pin) |




<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: (Reserved)Finger Print

| Size | Document Number | Rev |
|---|---|---|
| A4 | WASP 13" WHL-U | A 00 |

Date: Thursday, March 07, 2019 Sheet 92 of 106

WWW.AliSaler.Com

# (Blanking)

<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)*

| Size | Document Number | Rev |
|---|---|---|
| A4 | *WASP 13" WHL-U* | |

Date: Thursday, March 07, 2019 | Sheet 93 of 106

(Blanking)

<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
(Reserved)

| Size | Document Number | Rev |
|---|---|---|
| A 4 | WASP 13" WHL-U | A 00 |

Date: Thursday, March 07, 2019 Sheet 94 o f 106

WWW.AliSaler.Com

# (Blanking)

<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

*(Reserved)*

| Size | Document Number | Rev |
|---|---|---|
| A 4 | *WASP 13" WHL-U* | *A 00* |

Date: Thursday, March 07, 2019 Sheet 95 o f 106

# (Blanking)

<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

*(Reserved)*

| Size | Document Number | Rev |
|---|---|---|
| A 4 | *WASP 13" WHL-U* | *A 00* |

Date: Thursday, March 07, 2019 Sheet 96 o f 106

WWW.AliSaler.Com

(Blanking)

<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
*LVDS_Switch*

| Size | Document Number | Rev |
|---|---|---|
| A 4 | WASP 13" WHL-U | A00 |

Date: Thursday, March 07, 2019 Sheet 97 o f 106

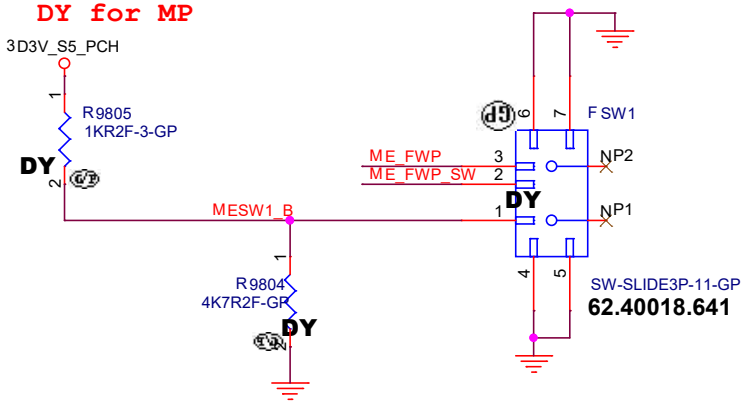
# Main Func = SWITCH

24 ME_FWP >>>

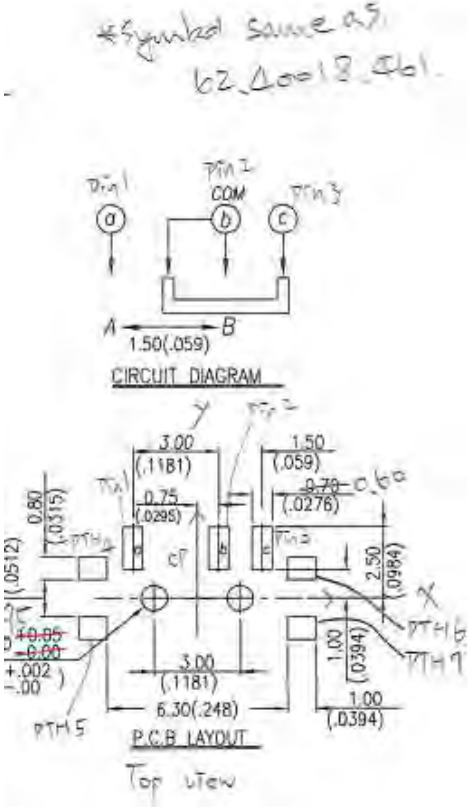
19 ME_FWP_SW <<<

## Firmware SW

**Default setting:pull LOW**
**DY for MP**




| | 3 | 1 |
|---|---|---|
| ME_FWP | LOW | HIGH |
| | Normal Operation (Default) | Override |




<Core Design>

**Wistron Corporation**
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CRT_Switch***

| Size | Document Number | Rev |
|---|---|---|
| A 4 | **WASP 13" WHL-U** | **A00** |

Date: Thursday, March 07, 2019 Sheet 98 of 106

WWW.AliSaler.Com

SSID = Debug

(Blanking)

<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

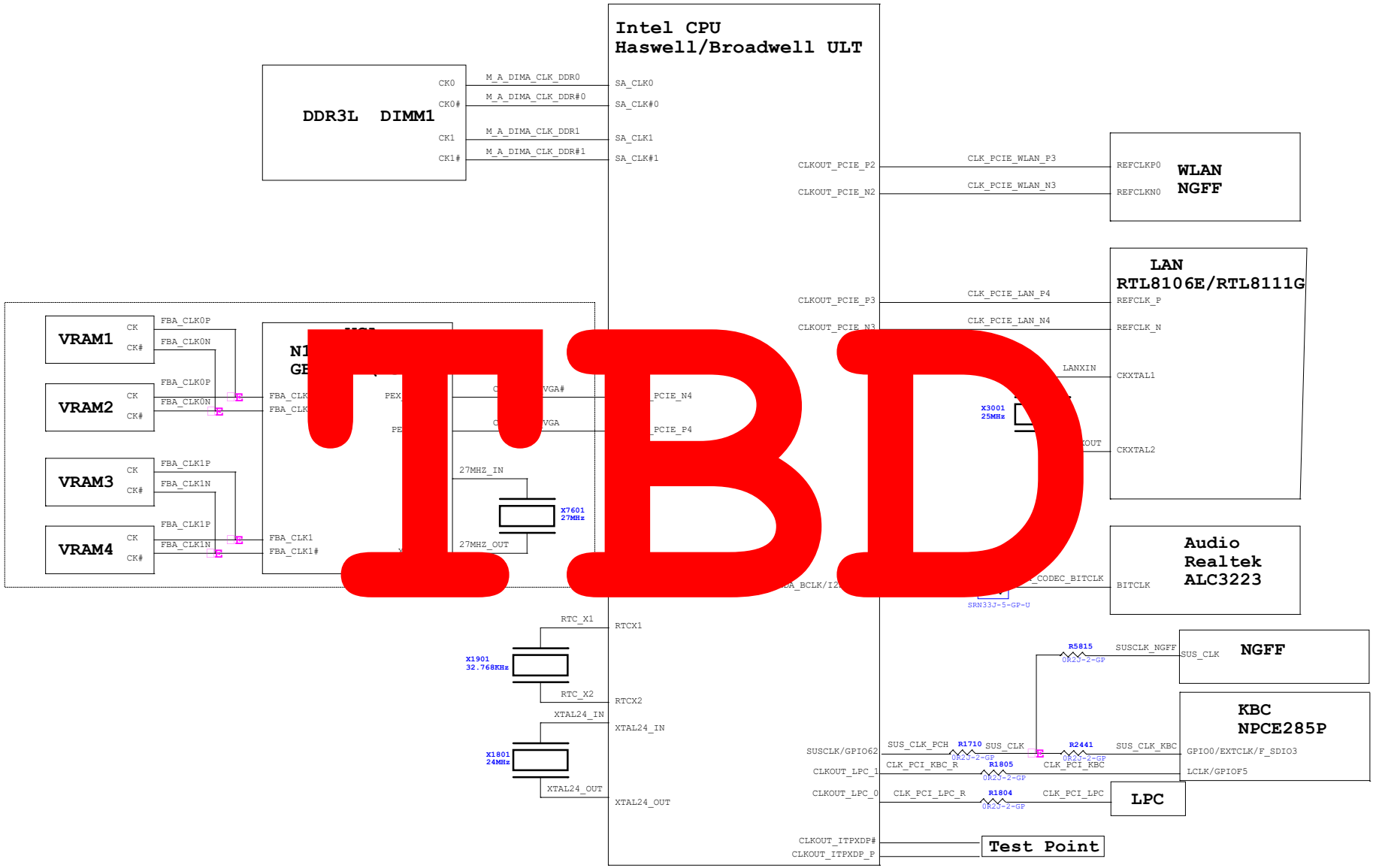
Title

*CPU_XDP;PCH_XDP*

| Size | Document Number | Rev |
|---|---|---|
| A 4 | WASP 13" WHL-U | A00 |

Date: Thursday, March 07, 2019 Sheet 99 o f 106

# CLK Block Diagram





<Core Design>
Wistron Corporation
3F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.


Title: CLK Block Diagram
Size: A | Document Number: WASP 13" WHL-U | Rev: A0
Date: Thursday, March 07, 2019 | Sheet 100 of 108

WWW.AliSaler.Com

*Change notes -*

| DATE | VERSON | DATE | Page | Modify List | OWNER |
|---|---|---|---|---|---|
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |

<Core Design>

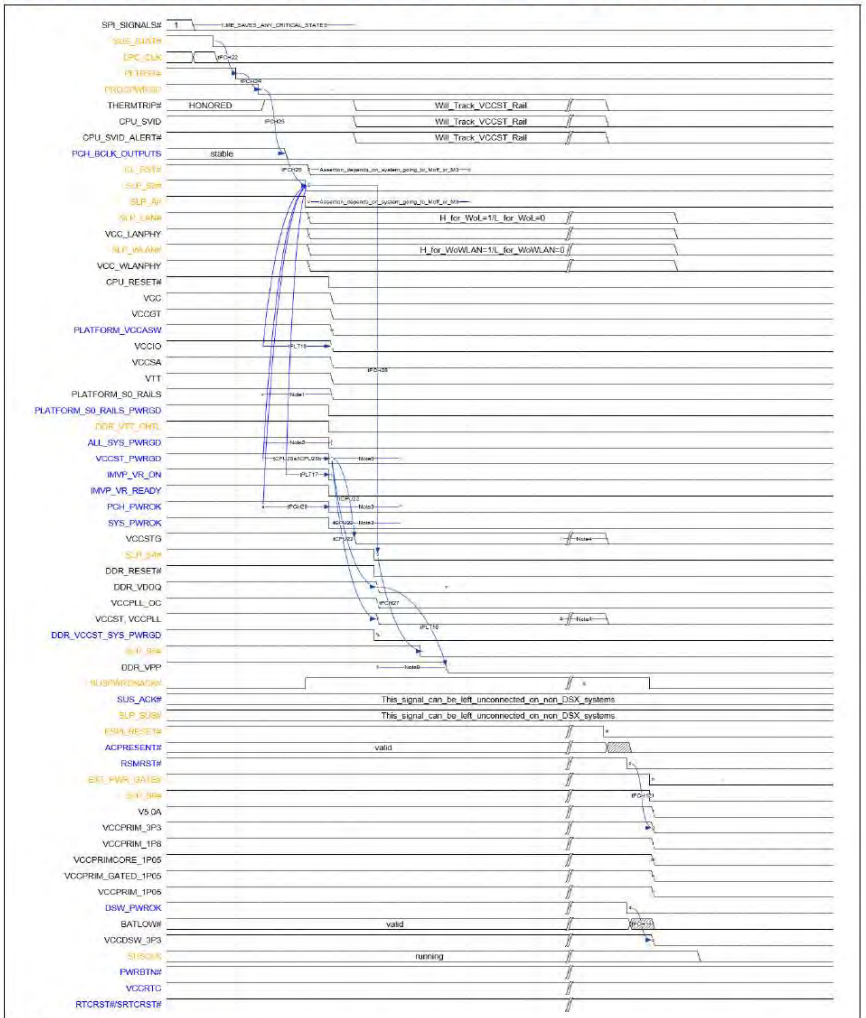
Wistron Corporation
2F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Change History*

Size: B | Document Number: *WASP 13" WHL-U* | Rev: *A00*

Date: Thursday, March 07, 2019 | Sheet 101 of 106

## Figure 12-21.WHL-U Timing Diagram for S0/M0 to G3 [Non Deep Sx Platform]




***Notes:***

1. These are all the processor S0 non-Core rails. Includes the rails like 3.3-V/5-V platform rails, etc.
2. This represents the overall Power-Good signal including the platform rails mentioned in Note (1)
3. Signal may drop before or after SLP _S4# / SLP_S5 # / DDR_RESET# assertion
4. VCCST, VCCSTG, and VCCPLL may remain powered during Sx power states for Debug support and platform VR optimization. Platform designers will need to account for proper power rail management with external devices and circuity to avoid leakage path scenarios.
5. VCCST_PWRGD signal must deassert in all Sx / DSx states, regardless of the status of the VCCST / VCCSTG rails
6. Present on LPDDR3 and DDR4 systems only. Must ramp down **AFTER** VDDQ has ramped down

<Core Design>

Wistron Corporation
3F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Power Sequence*

Size: A | Document Number: WASP 13" WHL-U | Rev: A0

Date: Thursday, March 07, 2019 | Sheet 102 of 106

WWW.AliSaler.Com

<Core Design>

Wistron Corporation
3F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Block Diagram

| Size | Document Number | Rev |
|---|---|---|
| A | WASP 13" WHL-U | A00 |

Date: Thursday, March 07, 2019 Sheet 103 of 108

<Core Design>

Wistron Corporation
3F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SMBUS Block Diagram

| Size | Document Number | Rev |
|---|---|---|
| A | WASP 13" WHL-U | A0 |

Date: Thursday, March 07, 2019 Sheet 104 of 108

<Core Design>

Wistron Corporation
3F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Audio Block Diagram

Size: A | Document Number: WASP 13" WHL-U | Rev: A0

Date: Thursday, March 07, 2019 | Sheet 105 of 108

<Core Design>

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

# CLK Block

| Size | Document Number | Rev |
|---|---|---|
| A 4 | WASP 13" WHL-U | A 00 |

Date: Thursday, March 07, 2019 Sheet 106 o f 106